GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (SIGNAL PROCESSING AND VLSI TECHNOLOGY) (26)

VLSI TEST PRINCIPALS AND ARCHITECTURES

SUBJECT CODE: 2732605

M.E. 3rd SEMESTER

Type of course: Introductory course for VLSI testing

Prerequisite: Nil

Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, various techniques for test pattern generation and various logic BIST techniques, etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks		Practical Marks				
L	T	P	C	ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
4	0	2#	5	70	30	20	10	10	10	150

Content:

Sr No	Course Content	Teaching hours	Module weightage
1	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	**5**	**9%**
2	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability	**12**	**21%**
3	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation	**11**	**20%**
4	**Test Generation:** Introduction, Random Test Generation, Theoretical Background: Boolean Difference, designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification, Designing a Simulation-Based ATPG, Advanced Simulation-Based ATPG, Hybrid Deterministic and Simulation-Based ATPG, ATPG for Non-Stuck-At Faults, Other Topics in test Generation.	**14**	**25%**
5	**Logic Built-In Self-Test:** Introduction, BIST Design Rule, Test Pattern Generation,Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement,BIST Timing /Control, Design Practice.	**14**	**25%**

Reference Books:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001

Course Outcome:

1 To realize importance and challenges of VLSI Testing at different abstraction levels.
2 To study and apply various fault models for generation of test vectors.
3 To calculate observability and controllability parameters of given circuit.
4 To study techniques to improve testability of a given circuit.
5 To convert a given circuit into a scan design.
6 To apply concepts of logic simulation and fault simulation in designing and testing of VLSI circuits.
7 To apply various algorithms for test pattern generation.
8 To study and analyze effect of logic built in self test (a DFT technique) in VLSI circuits designing.

List of Experiments:

1 Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
2 Write a VHDL/Verilog code to realize functioning of control Point Insertion technique.
3 Write VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered muxed-D scan cell.
4 Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
5 Write a VHDL/Verilog code to realize functioning of LSSD double latch design
6 Write a VHDL/Verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain
7 Write a VHDL/Verilog code to realize functioning of Linear feedback shift register.
8 Write a VHDL/Verilog code to realize functioning of built-in logic block observer.
9 Write a VHDL/Verilog code to realize functioning of Fixing bus contention in scan design rules.
10 Write a VHDL/Verilog code to realize functioning of Adding a lock-up latch between cross-clock-domain scan cells.

Open Ended Problems:

1 Write a C Program to calculate observability and controllability parameters of given circuit.
2 Write a C Program to generate test vectors for stuck at faults for a given combinational circuit.
3 Write a C Program to generate test vectors for transistors faults for a given circuit.
3 Write a C Program for Genetic algorithm.
4 Write a C Program for D algorithm.
5 Write a C Program for PODEM algorithm.
6 Design a one hot encoder for testing a tristate bus with four independent tristate drivers in BIST

mode.

7 Design X bounding circuit for improving the fault coverage of a bidirectional I/O port by forcing it to input mode during BIST operation.

List of Open Source Software/ Learning website:

1. ngspice/xilinx (software)
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.