GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (SIGNAL PROCESSING AND VLSI TECHNOLOGY) (26)

LOW POWER CMOS VLSI CIRCUIT DESIGN

SUBJECT CODE: 2732604

M.E. 3rd SEMESTER

Type of course: CMOS circuit design addressing Low power issues

Prerequisite: Basic knowledge of MOSFET, CMOS circuits

Rationale: This course provides a platform for students to analyze working of low power digital circuits like adders, multiplier, ROM, RAM, DRAM and systems. This is one of the advanced courses which will develop knowledge related to power dissipation issues in electronic systems and possible solutions to circumvent them.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks		Practical Marks				
L	T	P	C	ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
4	0	2#	5	70	30	20	10	10	10	150

Content:

Sr No	Course Content	Teaching hours	Module weightage
1	**Low – Power CMOS VLSI Design :** Introduction, Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation, Conclusions	**4**	**7**
2	**Circuit Techniques for Low – Power Design:** Introduction, Designing for Low – Power, Circuit Techniques for Power Reduction, Conclusions	**3**	**6**
3	**Low – Power CMOS Logic Circuits:** Introduction, Overview of Power Consumption, Low – Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits Exercise Problems	**8**	**14**
4	**Low Voltage Low – Power Adders:** Introduction, Standard Adder cells, CMOS Adder's Architectures, BICMOS Adder, Low – voltage Low – Power Design Techniques, Current – Mode Adders, Conclusions	**9**	**17**
5	**Low Voltage Low – Power Multipliers:** Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh – Wooley Multiplier, Booth Multiplier, Wallace Tree Multiplier, Conclusions	**9**	**17**
6	**Low Voltage Low – Power Read – Only Memories:**	**7**	**12**

	Introduction, Types of ROM, Basic Physics of Floating Gate Nonvolatile Devices, Floating Gate Memories, Basics of ROM, Low – Power ROM Technology, Future Trend and Development of ROMs, Conclusions		
7	**Low Voltage Low – Power Static Random–Access Memories:** Introduction, Basic of SRAM, Memory Cell, Precharge and Equalization circuit, Decoder, Address Transition Detection (ATD), Sense Amplifier, Output Latch, Low – Power SRAM Technologies, Future Trend and Development of SRAM, Conclusions	**7**	**12**
8	**Low Voltage Low – Power Dynamic Random – Access Memories:** Introduction, Types of DRAM, Basics of DRAM, Self – Refresh Circuit, Half – Voltage Generator (HVG), Back – Bias Generator (BVG), Boosted-Voltage Generator (BVG), Reference – Voltage Generator (BVG), Voltage –Down Converter (VDC), Future Trend and Development of DRAM, Conclusions	**7**	**12**
9	**Large Low – Power VLSI System Design and Applications:** Behavioral Level Transforms, Algorithm and Architecture Level Transforms for Low Power, Multiple and Dynamic Supply Design, Gated Clocking, Conclusions	**2**	**3**

Reference Books:

1. Low- Voltage, Low Power, VLSI Subsystems, Kiat-Seng Yeo ,Kaushik Roy, TATA McGraw-HILL EDITION.
2. CMOS Digital Integrated Circuits, 3rd Edition, Sung-Mo Kang, Yusuf Leblebici , TATA McGraw-HILL EDITION.
3. Low-Power Cmos Vlsi Circuit Design by Kaushik Roy, Sharat C. Prasad, Willey India Edition Low-power CMOS design, Anantha P. Chandrakasan, IEEE press

Course Outcome:

1. To study and understand basic concepts of static power consumption in CMOS circuits.
2. To study and understand the techniques for the power reduction.
3. To study and understand the effects of voltage scaling on low power circuits.
4. To analyze adiabatic logic circuit.
5. To analyze the basic principle, operation and application of CMOS adder, BICMOS adder and current mod adders.
6. To analyze the basic principle, operation and application of Braun Multiplier, Baugh – Woolley Multiplier, Booth Multiplier and Wallace Tree Multiplier.
7. To analyze the basic principle, operation and application of Floating Gate Memories and low power ROM circuits.
8. To analyze the basic principle, operation and application of low power SRAM circuits.
9. To analyze the basic principle, operation and application of Precharge and Equalization circuit, sense amplifier and decoder circuits.
10. To analyze the basic principle, operation and application of self refreshing circuits of DRAM memories.
11. To analyze the basic principle, operation and application of low power DRAM circuits.

List of Experiments:

1. To obtain leakage current of MOSFET devices for following technology:
    a. 250 nm
    b. 180 nm
    c. 90 nm
2. To obtain various power dissipation components in CMOS Inverter circuit for various technologies.
3. To simulate CMOS Inverter circuit using adiabatic logic concept and obtain power dissipation.
4. To implement and analyze two 4 bit adder without using XOR Gate.
5. To implement and analyze XOR/XNOR gate using following method:
    A. Dual rail domino logic style
    B. DPL
6. To implement and analyze shared BL 8T SRAM cell.
7. To implement and analyze 6T SRAM cell.
8. To implement and analyze 1 bit DRAM cell.
9. To implement and analyze bit line precharge using NMOS loads.
10. To implement and analyze bit line precharge using PMOS loads.
11. To implement and analyze operation of Half swing pulse mode AND gate.
12. To implement and analyze operation of reference voltage generator.
13. To implement and analyze charge pump circuit using hybrid pumping.
14. To implement and compare full adder using different methods.
15. To implement and analyze operation of sense amplifier for SRAM cell.

Open Ended Problems:

1. Simulate stacking effect in 2- input NOR gate.
2. Design NAND gate realization of the single-rail domino logic.
3. Design load less CMOS 4T SRAM cell using NgSpice.
4. Design ATD (Address Transition Detection) circuit using NgSpice.
5. Compare all types of sense amplifiers.
6. Design and compare 1T DRAM and SRAM using NgSpice.
7. Design two-phase back-bias generator.
8. Design and implement conventional CMOS full adder and modified CMOS full adder. Compare the speed between these two full adders.

Major Equipments: Function Generator, Power Supply, Multimeter, Digital Storage Oscilloscope

List of Open Source Software/learning website:

Ng-spice/Multisim
www.nptel.com
www.nptel.ac.in

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically

study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.