C-DAC &Gujarat Technological University
M.E. Electronics & Communication Engineering
(VLSI & Embedded Systems Design)
Gandhinagar

Semester: I

Subject Name: Digital VLSI Design & Verification–I Frontend(Elective-I)

Subject Code: 2715204

UNIT – I Basics of Semiconductor Devices
P-N junction & BJT structure and principle of operation, Device Modeling Introduction to Device modeling, numerical methods and meshing (fixed and adaptive). Numerical solutions, common methods – Newton, Gummel. IV characteristics and parametric extraction. Gate currents

UNIT – II Introduction - Levels of IC design – Digital circuit fundamentals
Concept of IC. IC structure, components, applications. History and evolution of the IC industry. Moore's Law. Design economics - Nonrecurring engineering costs (NRE) & Recurring costs, Yield & Technology scaling. System level Design. Top down design. Bottom up design. Back end design. Design abstraction levels. Behavior Level. Register-Transfer Level (RTL). Logic Level. Circuit
Level. Component level. Examples of Domains and its Abstraction Levels. CMOS logic gates, Combinational circuits, Sequential circuits, FSM

UNIT – III Design Flow
Design flow: Frontend – Marketing Requirements, Design specification, Verification plan, RTL description, Functional verification, Synthesis. Backend – Partitioning, Floor planning, Placement, CTS, Routing & layout generation, layout verification, Tapeout. Foundry – Fabrication Introduction to Testing – Need for testing, manufacturing test, design for test, chip-level test, system-level test, test generation & fault models Introduction to System on chip (Soc) design - Soft cores, Firm cores, Hard cores. Study of AMBA AXI4 protocol.

UNIT – IV IC Design techniques & options, CAD design, Design challenges
Structured design techniques: hierarchy, regularity, modularity, locality. Design options: Programmable logic Design, sea of gates and gate array design, standard cell design, full-custom design. Study of FPGA tools. Using of CAD tools: Behavioral synthesis tool, RTL synthesis tool , logic optimization tool, structural to layout synthesis tool, layout synthesis tool, design capture tools, design verification tools, circuit extractor, design rule checker (DRC), electrical rule checker (ERC), layout vs. schematic.
Design challenges – Microscopic issues: ultra-high speeds, power dissipation, supply rail drop, importance of inter connect, noise, crosstalk, reliability, manufacturability, clock distribution
Macroscopic issues: time to market, design complexity, high levels of abstractions, reuse, IP, portability, tool interoperability. Sub-nm technologies: technology scaling, switching power reduction, leakage power control, process variations, die to die frequency variation, temperature variation.

UNIT – V Digital Design and Synthesis

VHDL and Verilog HDL. Concepts of Design planning, partitioning, RTL design for Sequential & combinational circuits, State machines design & encoding. Simulation , waveform generation, coverage reports. Synthesis concepts, Technology libraries, Constraints, Netlist generation & optimization.

UNIT – VI System Verilog understanding

Data types, Attributes, Procedural Statement, Control flow, Operators & Expressions
Process, Task & Functions, Classes & OOP concepts, Random generation, constrains, Inter process communication, Clocking blocks, Programming blocks, Assertions, Its use in Design and Verification, Functional Coverage, Direct Programming Interface, Verification Using System Verilog.

Lab:

Tools used during laboratory works: VCS/Modelsim & Design Compiler/Xilinx ISE
Study and implementation using VCS/Modelsim and Design Compiler/Xilinx ISE

Reference:

1. Silicon Processing for the VLSI Era, S. Wolf, and R.N. Tauber, ISBN0-9616721-6-1, Lattice Press, Sunset Beach (2000)
2. Synopsys recommended course material and lectures.
3. N. Weste, K. Eshragyan. Principles of CMOS VLSI Design. Adisson Wesley, 1993
4. J.F. Wakerly. Digital Design - Principles & Practices, Prentice Hall, 2001
5. Digital logic design by Morris Mano
6. Verilog HDL: A guide to digital design & synthesis, 2e by Samir Palnitkar
7. IEEE Std 1364™-2005 - Verilog LRM
8. System Verilog LRM.