GUJARAT TECHNOLOGICAL UNIVERSITY

POWER ELECTRONICS (24)
PROGRAMMABLE LOGIC DEVICES & APPLICATIONS
SUBJECT CODE: 2162412
B.E. 6th SEMESTER

Type of Course: Engineering Science (Electronics)

Prerequisite: 2142406 (Digital Electronics & its Applications)
2152409 (Micro Controller for Power Electronics)

Rationale: This subject is aimed at developing concept of implementation of digital systems using programmable logic devices, digital I/O, interfacing with real world etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks			Practical Marks			
L	T	P	C	ESE (E)	PA (M)		PA (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	150

Content:

Sr. No.	Topic With Details	Teaching Hrs.	Module Weightage
1	**Introduction:** Review of combinational logic design, sequential logic design, Overview of embedded systems, design challenges, processor technology, IC technology, design technology, trade offs	6	15
2	**General purpose Processors**: Introduction, Basic architecture, Operation, Programmer's view, Development environment, Application Specific Instruction set Processors (ASIPs), Selecting a microprocessor	4	10
3	**Single-Purpose Processors:** Combinational logic, sequential logic, custom single purpose processor design, R-T level custom single purpose processor design, Optimizing design, General purpose processor design, Timers, counters, watch dog timers, UART, Pulse Width Modulators, LCD controllers, Keyboard controllers, Stepper motor controllers, Analog-to- Digital converters, RTC	8	15
4	**Memory**: Memory write ability, storage permanence, memory types, composing memory, memory hierarchy, cache, SRAM, DRAM, EDO DRAM, SDRAM, RDRAM etc., Memory management unit	6	10
5	**Programmable Logic Devices**: PAL, PLA, FPGA, CPLD etc. , FPGA based system design, FPGA architecture, Programmable logic device manufacturers and their devices	6	10
6	**Hardware Description Language**: Concept of hardware description languages like Verilog, VHDL etc., logic design process, modeling with HDL, Structural, data flow and behavioral modelling, Concept of network delay, power and energy optimization etc.	8	10
7	**Implementation of Logic Circuits using HDL**: Implementation of combinational circuits, sequential machine design, Finite State Machine etc. using HDL	8	15
8	**Simulation, modelling and implementation tools:** Xilinx ISE, Vivado, Altera Quartus II etc., Use of the software for design, simulation, design verification, placement, verification , test bench etc.	6	10

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks (%)					
R Level	U Level	A Level	N Level	E Level	C Level
30%	**25%**	**25%**	**10%**	**10%**	**0**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Embedded System Design A Unified Hardware Software Introduction, Frank Vahid, Tony Givargis, Wiley India
2. FPGA based system design , Wayne Wolf, Pearson
3. A VHDL Primer, J Bhaskar, Pearson
4. A Verilog HDL Primer, J Bhaskar
5. A VHDL Synthesis Primer, J. Bhaskar

Course Outcome:

After learning this course, the students should be able to understand following concepts.

1. Importance of programmable logic devices in implementing real systems.
2. Programmable logic devices and implementation of logic through PLD
3. Designing simple FSM for simple systems
4. Design flow, simulation and design tools used, working with these tools etc.

Laboratory Work:

Objectives: The laboratory work is aimed at putting the theory learnt in class in practice and to show the results are nearly matched with theory. In this context, following are the core objectives for laboratory work of this subject.

- Develop understanding of basics of programmable logic devices.
- Understand the basics of design flow of digital systems using PLD
- Develop understanding of digital design.
- Understand the use Verilog/VHDL for simulation, synthesis and implementation of digital system.
- Concept of using any one tool for PLD development tool

Directions for Laboratory work:

- ✓ The list of experiments is given as a sample.
- ✓ Minimum 10 experiments should be carried out. Alternatively, around 7 experiment for basic study should be given. Based on basic study, a small digital system modelling exercise can be given. e.g. PWM generator,
- ✓ Similar laboratory work fulfilling the objectives can also be considered.
- ✓ As far as possible printed manual should be preferred so that students can concentrate in laboratory experiments and related study.

The sample list of experiments is given below with reference to VHDL and

List of Practical and Open Ended Problems:

1. Study of Design flow for digital logic design using HDL
2. Study of VHDL
3. Study of Xilinx ISE Web pack software
4. To model and simulate simple combinational circuits.

5. To model and simulate a 1 bit full adder and 4 bit parallel adder.
6. To model and test simple sequential circuit (e.g. binary up/down counter) using FSM (Mealy / Moore)
7. To model and simulate memory
8. To model and simulate a single purpose processor. (This is having weightage of 3 experiments. This experiment should be given in group of 2-3 students. Each group should be assigned a separate single purpose processor. The examples are watch dog timer, PWM, 7 segment display controller, key board interface, GCD, binary multiplier etc.)

List of Open Source Software/learning website:

Open Source Software:

- ISE webPACK → http://www.xilinx.com/

Web-base tools for design:

- Quartus II Web Edition → https://www.altera.com

Open source for Math Tools:

- http://maxima.sourceforge.net/
- http://www.sagemath.org/
- http://www.scilab.org/
- http://www.gnu.org/software/octave/

Learning website:

- http://nptel.iitm.ac.in/courses.php
- http://ocw.mit.edu/
- http://www.electrical-engineering-portal.com
- http://www.fpga4fun.com/
- http://www.eng.auburn.edu/department/ee/mgc/vhdl.html
- http://allaboutfpga.com/
- http://www.iverilog.com/
- http://www.edaplayground.com/
- http://www.asic-world.com/
- http://www.gmvhdl.com/

Major Equipments:

- Oscilloscope, Logic Analyser, Multimeter, FPGA kit etc.
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Active learning Assignments (AL) : Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.