GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS (10)
VLSI DESIGN
SUBJECT CODE: 2161004
B.E. 6thSEMESTER

Type of course: CMOS VLSI Design**.**

Prerequisite: Basic electronics, Digital design

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks			Practical Marks			
				ESE (E)	PA (M)		ESE (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Introduction** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, ,computer aided design technology	2	10%
2	**Fabrication of MOSFET :** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	4	10%
3	**MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances	8	20%
4	**MOS Inverters: Static Characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter	7	15%
5	**MOS Inverters Switching characteristics and Interconnect Effects :** Introduction, Delay-time definitions, Calculation of Delay times, Inverter designwith delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters	8	15%
6	Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs)	5	10%
7	Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocke dlatch and Flip-flop circuit, CMOS D-latch and Edge-triggered	4	10%

	flip-flop		
8	Introduction, Fault types and models, Controllability and observability, AdHoc Testable design techniques, Scan –based techniques, built-in SelfTest (BIST) techniques, current monitoring IDDQ test	**3**	10%

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10%	**20%**	**20%**	**20%**	**15%**	**15%**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf
2. Leblebici, TATA McGraw-Hill Pub. Company Ltd., Third Edition.
3. Basic VLSI Design By Pucknell and Eshraghian, PHI,3rd ed.
4. CMOS circuit design, layout and simulation By R. Jacob Baker, Harry W. Li and David E. Boyce.
5. Chip Design for Submicron VLSI :CMOS layput and Simulation by John P Uyemura, THOMSON INDIA EDITION

Course Outcome:

After learning the course the students should be able to:

1. CMOS VLSI design concepts
2. Work with various EDA tools used in chip design process.
3. Design layput for back-end.
4. CMOS based design analysis.

List of Experiments:

1. Introduction to layout design software.
2. To study N-MOS and I-V characteristics.
3. To study P-MOS and I-V characteristics.
4. To study CMOS transfer characteristics.
5. To study CMOS based circuit simulation.
6. To study designing of CMOS inverter layout.
7. To study designing of AND gate and simulation.
8. To study designing of OR gate and simulation.
9. To study designing of Half adder gate and simulation.
10. To study designing of 2x1 Multiplexers and simulation.
11. To study designing of Analog circuits using SPICE.

Design based Problems (DP)/Open Ended Problem:

1. Amplifier design.
2. Comparator design.
3. Current Mirror design.
4. Six transistor SRAM design.
5. ROM Memory design.

Major Equipment:

1)Microwind
2)Tanner
3)Ngspice
4)Magic

List of Open Source Software/learning website:

1)Ngspice
2)Magic

ACTIVE LEARNING ASSIGNMENTS: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.