# GUJARAT TECHNOLOGICAL UNIVERSITY

**ELECTRONICS (10)**
DIGITAL DESIGN
**SUBJECT CODE:** 2151007
B.E. 5th SEMESTER

**Type of course:** Front end chip design process through HDL

**Prerequisite:** Digital Logic Design

**Rationale:** Chip design is a computer aided design process in current scenario. To design chip now a day's industry prefers to test it carefully on computer aided software tools. The software tools support hardware descriptive language (HDL) compiler. The chip designer can able to program and test the programs on simulator. The front end design can also, be tested on FPGA/CPLD development kits.

**Teaching and Examination Scheme:**

| Teaching Scheme | | | Credits | Examination Marks | | | | | | Total Marks |
|---|---|---|---|---|---|---|---|---|---|---|
| L | T | P | C | Theory Marks | | | Practical Marks | | | |
| | | | | ESE (E) | PA (M) | | ESE (V) | | PA (I) | |
| | | | | | PA | ALA | ESE | OEP | | |
| 4 | 0 | 2 | 6 | 70 | 20 | 10 | 20 | 10 | 20 | 150 |

**Content:**

| Sr. No. | Content | Total Hours | %Weight |
|---|---|---|---|
| 1 | Introduction to digital design. Introduction to hardware descriptive language (HDL). Difference between computer programming languages and HDLs Examples and HDL based digital design flow based on FPGA and CPLD. | 5 | 10 |
| 2 | Basic concepts of HDL (Verilog/VHDL), Level of abstractions supported by HDLs, Data types and syntaxes of HDLs. Instantiation concepts. Switch level modeling and its example, | 8 | 10 |
| 3 | Structural modeling, Component declaration, component instantiation, Generics and Configuration. Packages and libraries, Gate level modeling and its example, Dataflow level modeling and its example. | 10 | 20 |
| 4 | Behavioral Level modeling:<br>Entity declaration, Architecture body, process statement, variable and signal assignment statements, Wait statements, If statements, case statements, Loop statements etc. | 10 | 20 |
| 5 | User Defined Primitives (UDPs) and its examples, Finite State Machine (FSM) implementation by HDL, FSM implementation example in HDL. | 5 | 10 |
| 6 | Synthesis and simulation of combinational and sequential logic, FPGA and CPLD based Implementation. | 6 | 15 |

| | | | |
|---|---|---|---|
| 7 | Hardware modeling examples: ALU, Binary multiplier, Pulse counter, Barrel shifter, UART, Traffic light controller, DRAM Model etc. | 10 | 15 |

**Suggested Specification table with Marks (Theory):**

| **Distribution of Theory Marks** | | | | | |
|---|---|---|---|---|---|
| R Level | U Level | A Level | N Level | E Level | C Level |
| **10 %** | **20%** | **20%** | **20%** | **15%** | **15%** |

**Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)**

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

**Reference Books:**


1) Verilog HDL A Guide to Digital Design and Synthesis, By Samir Palnitkar Publication: Pearson Education
2) VHDL Primer, By J. Bhaskar, Publication: PHI


**Course Outcome:**

After learning the course the students should be able to:

1) Work with Hardware Descriptive Language like Verilog/VHDL.
2) Work with various EDA tools used in chip design process.
3) Work with EDA tools of VLSI.
4) Test and analysis of digital design on simulator that support HDL compiler.
5) Verification of soft code implemented in HDL through verification tools.
6) Implement various digital logic blocks on FPGA/CPLD boards.
7) System design and implementation on FPGA/CPLD boards.
8) Develop project based on FPGA/CPLD through HDL language.

**List of Experiments:**

1. Introduction to HDL language Verilog/VHDL
2. Implement basic digital logic gates and simulate with HDL.
3. Design and implement half adder logic with HDL and simulate the same.
4. Design and implement full adder logic with HDL and simulate the same.
5. Design and implement fast adder logic with HDL and simulate the same.
6. Design and implement multiplexers with HDL and simulate the same.
7. Design and implement multiplier with HDL and simulate the same.
8. Design and implement 4-bit counter with HDL and simulate the same.
9. Multiplier logic with HDL and simulate the same.
10. Design and simulate the Finite State Machine (FSM) design by HDL.
11. Design and simulate the ALU design by HDL.

**Design based Problems (DP)/Open Ended Problem:**

1) Implement the design of 3-bit ALU on simulator.
2) Implement BCD counter on simulator and FPGA.
3) Implement memory on FPGA and test by data read and write.

**Major Equipment:**

1) Electronic Design Automation (EDA) Tools.
2) FPGA/CPLD Development kits.
3) HDL simulator and compiler tools

**List of Open Source Software/learning website:**

1) www.xilinx.com, Xilinx project navigator evaluation tools version.
2) www.altera.com, Altera Quartus evaluation software tool.

**ACTIVE LEARNING ASSIGNMENTS**: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.