

GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering (VLSI System Design Engineering)

Semester – II

Subject Code: 1724206

Subject Name: Electronics System Level Design (Institute Elective –II)

Sr. No.	Course Content
1	Introduction
2	System Level Design: System Specification, Design Space Exploration, SoC, Multiprocessor design using Configurable Processor, System Performance acceleration, Performance Modeling.
3	System Level Modeling: Transactional Level Modeling, System C
4	System Level Verification: System Verilog
5	System Level Techniques for Power Optimization: Low Power SOC Design, System Level Memory exploration and optimization, performance Analysis of Memory subsystem

Text/References:

1. Mark D. Birnbaum “Essential Electronics Design Automation” 2004
2. Pierre Boulet “Advanced in Design and Specification Languages for SOCS”,2005 Selected Contributors
3. IEEE Transactions/Journals, Research papers/Conferences/Workshops in Electronics Level Design and EDA Tools