

# GUJARAT TECHNOLOGICAL UNIVERSITY

## Master of Engineering (VLSI System Design Engineering)

### Semester – II

**Subject Code:** 1724202

**Subject Name:** Testing and Verification of VLSI Design

Sr. No.	Course Content
1	Introduction
2	Testing Combinatorial Circuits
3	Testing Sequential Circuits
4	Random Pattern Testing, Memory Testing
5	Analog and Mixed Signal Testing
6	Delay Testing; IDDQ Testing
7	DFT Techniques; BIST Techniques
8	Boundary Scan Architecture and Testing, Functional and Formal Verification
9	SoC and Embedded System Testing; Future Trends.

**Laboratory work:** It will consist of 10 to 12 experiment based on above syllabus.

#### Text/References:

1. M.L.Bushnell and V.D.Agrawal,Essentials of Electronic testing for Digital.Memory and Mixed Signal VLSI Circuits,Kluwer,2000.
2. M. Abramovici,M.A. Breuer and A.D. Friedman,Digital Systems Testing and Testabel Design,Wiley/IEEE press,-2000.
3. A.Miczo,Digital Logic Test and Simulation,Second Edition,Wiley,2003.
4. S.Mourad and Y.Zorian,Principles of testing Electronic Systems,Wiley,2000.
5. A.L.Crouch,Design for Test for Digital ICs and Embedded core Systems,PH,2000.
6. R.Rajsuman,System-on-a-Chip Design and Test,Artech,2000.
7. B.Vinnakota, Analog and Mixed-Signal Test,PH,1998.
8. K.P.Parker,The Boundary Scan Handbook,Third Edition,Kluwer,2003.
9. V.Agrawal andb S.C.Seth,Test Generation for VLSI Chips,IEEE CS Press,1989.
10. Writng testbenches functional verification of HDL models by Janick Bargeron.