GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering (VLSI System Design Engineering)

Semester – II

Subject Code: 1724201

Subject Name: Power Efficient VLSI Design

Sr. No.	Course Content
1	Introduction
2	Need for Low Power VLSI Chips, Sources of Power dissipation on Digital Integrated circuits. Emerging Low Power Approaches. Physics of Power dissipation in CMOS Devices. Device and Technology Impact on low Power designs.
3	Dynamic dissipation in CMOS, Transistor sizing and gate oxide thickness, impact of technology Scaling, technology and device innovation.
4	Power estimation Simulation Power analysis SPICE circuit simulators, Gate Level Logic simulation, Capacitive power estimation, static state power, gate level capacitance estimation, Architecture level analysis, Data correlation analysis in DSP System. Montecarlo Simulation. Probabilistic Power Analysis: Random Logic Signals, Probability and frequency, Probabilistic Power Analysis techniques, Signal entropy.
5	Low Power Design: Circuit level: Power consumption in circuits. Flip-flops and latches design, High capacitance nodes, low power digital cells library logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.
6	Low Power Architecture and Systems: Power and Performance Management, Switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
7	Low power Clock Distribution : Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co design of clock network
8	Algorithm and architected level methodologies: Introduction, design flow, Algorithmic level analysis and optimization, Architectural level estimation and synthesis.

Texts/References:

1. Gray K. Yeap," Practical Low power Digital VLSI Design ", KAP,2002
2. Rabaey, Pedram, "Low power Design methodologies" Kuwer Academic, 1997
3. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit " Wiley,2000
4. Kaushik Roy, Kait-SengYo, Low Voltage Low Power VLSI Subsystems, TMH