Chapter No. 3
Differential Amplifiers

Operational Amplifiers:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MH Z to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

Such direct coupled (dc) amplifiers do not use blocking (coupling and by pass) capacitors since these would reduce the amplification to zero at zero frequency. Large by pass capacitors may be used but it is not possible to fabricate large capacitors on a IC chip. The capacitors fabricated are usually less than 20 pf. Transistor, diodes and resistors are also fabricated on the same chip.

Differential Amplifiers:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals.

How the differential amplifier is developed? Let us consider two emitter-biased circuits as shown in fig. 1.

![Fig. 1](image)

The two transistors Q₁ and Q₂ have identical characteristics. The resistances of the circuits are equal, i.e. \( R_{E1} = R_{E2}, R_{C1} = R_{C2} \) and the magnitude of \( +V_{CC} \) is equal to the magnitude of \( -V_{EE} \). These voltages are measured with respect to ground.

To make a differential amplifier, the two circuits are connected as shown in fig. 1. The two \( +V_{CC} \) and \( -V_{EE} \) supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of \( R_{E1} \) and \( R_{E2} \) is replaced by a resistance \( R_{E} \). The two input signals \( v_1 \) & \( v_2 \) are applied at the base of Q₁ and at the base of Q₂. The output voltage is taken between two collectors. The collector
resistances are equal and therefore denoted by \( R_C = R_{C1} = R_{C2} \).

Ideally, the output voltage is zero when the two inputs are equal. When \( v_1 \) is greater than \( v_2 \) the output voltage with the polarity shown appears. When \( v_1 \) is less than \( v_2 \), the output voltage has the opposite polarity.

The differential amplifiers are of different configurations.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
These configurations are shown in **fig. 2**, and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

**Dual Input, Balanced Output Differential Amplifier:**

The circuit is shown in **fig. 1**, $v_1$ and $v_2$ are the two inputs, applied to the bases of $Q_1$ and $Q_2$ transistors. The output voltage is measured between the two collectors $C_1$ and $C_2$, which are at same dc potentials.

**D.C. Analysis:**

To obtain the operating point ($I_{CC}$ and $V_{CEQ}$) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages $v_1$ and $v_2$ to zero as shown in **fig. 3**.

![Fig. 3](image)

The internal resistances of the input signals are denoted by $R_S$ because $R_{S1} = R_{S2}$. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of $I_{CQ}$ and $V_{CEQ}$ can be used for second transistor $Q_2$.

Applying KVL to the base emitter loop of the transistor $Q_1$.
The value of $R_E$ sets up the emitter current in transistors $Q_1$ and $Q_2$ for a given value of $V_{EE}$. The emitter current in $Q_1$ and $Q_2$ are independent of collector resistance $R_C$.

The voltage at the emitter of $Q_1$ is approximately equal to $-V_{BE}$ if the voltage drop across $R$ is negligible. Knowing the value of $I_C$ the voltage at the collector $V_C$ is given by

$$V_C = V_{CC} + I_C R_C$$

and $V_{CE} = V_C + V_E$

$$= V_{CC} + I_C R_C + V_{BE}$$

$$V_{CE} = V_{CC} + V_{BE} + I_C R_C \quad (E-2)$$

From the two equations $V_{CEQ}$ and $I_{CQ}$ can be determined. This dc analysis applicable for all types of differential amplifier.

**Example - 1**

The following specifications are given for the dual input, balanced-output differential amplifier of **fig.1**: $R_C = 2.2 \text{ k}\Omega$, $R_B = 4.7 \text{ k}\Omega$, $R_{in1} = R_{in2} = 50 \text{ } \Omega$, $+V_{CC} = 10 \text{ V}$, $-V_{EE} = -10 \text{ V}$, $\beta_{dc} = 100$ and $V_{BE} = 0.715\text{ V}$. Determine the operating points ($I_{CQ}$ and $V_{CEQ}$) of the two transistors.

**Solution:**

The value of $I_{CQ}$ can be obtained from equation (E-1).

$$I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}}$$

$$= \frac{10 - 0.715}{9.4 \text{ k}\Omega + \frac{50}{100}} = 0.988\text{ mA}$$
The voltage $V_{CEQ}$ can be obtained from equation (E-2).

\[
V_{CEQ} = V_{CC} + V_{BE} - R\cdot I_CQ
\]
\[
= 10 + 0.715 - (2.2k\Omega)(0.988mA)
\]
\[
= 8.54V
\]

The values of $I_{CQ}$ and $V_{CEQ}$ are same for both the transistors.

**Dual Input, Balanced Output Difference Amplifier:**

The circuit is shown in **fig. 1** $v_1$ and $v_2$ are the two inputs, applied to the bases of $Q_1$ and $Q_2$ transistors. The output voltage is measured between the two collectors $C_1$ and $C_2$, which are at same dc potentials.

![Fig. 1](image)

**A.C. Analysis:**

In previous lecture dc analysis has been done to obtain the operating point of the two transistors.

To find the voltage gain $A_d$ and the input resistance $R_i$ of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in **fig. 2**. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.
Since the two dc emitter currents are equal. Therefore, resistance \( r'_{e1} \) and \( r'_{e2} \) are also equal and designated by \( r'_{e} \). This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages \( v_1 \) and \( v_2 \). This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector \( C_2 \) is assumed to be more positive with respect to collector \( C_1 \) even though both are negative with respect to to ground.

Applying KVL in two loops 1 & 2.

\[
\begin{align*}
    v_1 &= R_{S1} i_{b1} + i_{e1} r'_{e} + (i_{e1} + i_{e2}) R_E \\
    v_2 &= R_{S2} i_{b2} + i_{e2} r'_{e} + (i_{e1} + i_{e2}) R_E
\end{align*}
\]

Substituting current relations,

\[
\begin{align*}
    i_{b1} &= \frac{i_{e1}}{\beta}, \quad i_{b2} = \frac{i_{e2}}{\beta} \\
    V_1 &= \frac{R_{S1}}{\beta} i_{e1} + r'_{e} i_{e1} + R_E (i_{e1} + i_{e2}) \\
    V_2 &= \frac{R_{S2}}{\beta} i_{e2} + r'_{e} i_{e2} + R_E (i_{b1} + i_{e2})
\end{align*}
\]

Again, assuming \( R_{S1} / \beta \) and \( R_{S2} / \beta \) are very small in comparison with \( R_E \) and \( r'_e \) and therefore neglecting these terms,
Solving these two equations, \( i_{e1} \) and \( i_{e2} \) can be calculated.

\[
\begin{align*}
    i_{e1} &= \frac{(r'_e + R_E) v_1 - R_E v_2}{(r'_e + R_E)^2 - R_E^2} \\
    i_{e2} &= \frac{(r'_e + R_E) v_2 - R_E v_1}{(r'_e + R_E)^2 - R_E^2}
\end{align*}
\]

The output voltage \( V_O \) is given by

\[
V_O = V_{C2} - V_{C1}
\]

\[
= -RC i_{C2} - (-RC \cdot i_{C1})
\]

\[
= RC (i_{C1} - i_{C2})
\]

\[
= RC (i_{e1} - i_{e2})
\]

Substituting \( i_{e1} \), \( i_{e2} \) in the above expression

\[
v_o = RC \left\{ \frac{(r'_e + R_E) v_1 - R_E v_2}{(r'_e + R_E)^2 - R_E^2} \cdot \frac{(r'_e + R_E) v_2 - R_E v_1}{(r'_e + R_E)^2 - R_E^2} \right\}
\]

\[
= \frac{RC (v_1 \cdot v_2)}{r'_e (r'_e + 2R_E)}
\]

Therefore, \( v_o = \frac{RC}{r'_e} (v_1 \cdot v_2) \)  \hspace{1cm} (E-1)

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as \( v_d = v_1 - v_2 \) the voltage gain of the dual input balanced output differential amplifier can be given by

\[
A_d = \frac{v_C}{v_d} = \frac{RC}{r'_e} \hspace{1cm} (E-2)
\]

**Differential Input Resistance:**

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance \( R_{i1} \) seen from the input signal source \( v_1 \) is determined with the signal source \( v_2 \) set at zero. Similarly, the input signal \( v_1 \) is set at zero to determine the input resistance \( R_{i2} \) seen from the input signal source \( v_2 \). Resistance \( R_{i1} \) and \( R_{i2} \) are ignored because they are very small.
\[ R_{i1} = \frac{V_1}{b_1 v_2} = 0 \]
\[ = \frac{V_1}{b_1 \beta} v_2 = 0 \]

Substituting \( i_{c1} \),

\[ R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E} \]

Since \( R_E \gg r'_e \)
\[ \therefore r'_e + 2R_E \gg 2R_E \]
\[ \text{or} \quad r'_e + R_E \gg R_E \]
\[ \therefore R_{i1} = 2\beta r'_e \quad \text{(E-3)} \]

Similarly,

\[ R_{i2} = \frac{V_2}{b_2 v_1} = 0 \]
\[ = \frac{V_2}{b_2 / \beta} v_1 = 0 \]
\[ R_{i2} = 2\beta r'_e \quad \text{(E-4)} \]

The factor of 2 arises because the \( r'_e \) of each transistor is in series.

To get very high input impedance with differential amplifier is to use Darlington transistors. Another ways is to use FET.

**Output Resistance:**

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance \( R_{O1} \) measured between collector \( C_1 \) and ground is equal to that of the collector resistance \( R_C \). Similarly the output resistance \( R_{O2} \) measured at \( C_2 \) with respect to ground is equal to that of the collector resistor \( R_C \).

\[ R_{O1} = R_{O2} = R_C \quad \text{(E-5)} \]

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

**Example - 1**

The following specifications are given for the dual input, balanced-output differential amplifier: \( R_C = 2.2 \, \text{k}\Omega \), \( R_B = 4.7 \, \text{k}\Omega \), \( R_{in 1} = R_{in 2} = 50\Omega \), \(+V_{\text{CC}}= 10\, \text{V}\), \(-V_{\text{EE}} = -10\, \text{V}\), \( \beta_{dc} = 100 \) and \( V_{BE} = 0.715\, \text{V} \).
a. Determine the voltage gain.
b. Determine the input resistance
c. Determine the output resistance.

Solution:

(a). The parameters of the amplifiers are same as discussed in example-1 of lecture-1. The operating point of the two transistors obtained in lecture-1 are given below

\[ I_{CQ} = 0.988 \text{ mA} \]
\[ V_{CEQ} = 8.54 \text{ V} \]

The ac emitter resistance

\[ r_e' = \frac{25 \text{ mV}}{I_{E} \text{ mA}} = \frac{25 \text{ mV}}{0.988 \text{ mA}} = 25.3 \Omega \]

Therefore, substituting the known values in voltage gain equation (E-2), we obtain

\[ A_v = \frac{V_o}{V_{id}} = \frac{R_C}{r_e} = \frac{2.2 \text{ k} \Omega}{25.3} = 86.96 \]

b). The input resistance seen from each input source is given by (E-3) and (E-4):

\[ R_{i1} = R_{i2} = 2\beta_{ae}r_e = (2)(100)(25.3) = 5.06 \text{ k} \Omega \]

(c) The output resistance seen looking back into the circuit from each of the two output terminals is given by (E-5)

\[ R_{o1} = R_{o2} = 2.2 \text{ k} \Omega \]

A dual input, balanced output difference amplifier circuit is shown in fig. 1.
Inverting & Non? inverting Inputs:

In differential amplifier the output voltage $v_O$ is given by

$$V_O = A_d (v_1 - v_2)$$

When $v_2 = 0$, $v_O = A_d v_1$

& when $v_1 = 0$, $v_O = -A_d v_2$

Therefore the input voltage $v_1$ is called the non inverting input because a positive voltage $v_1$ acting alone produces a positive output voltage $v_O$. Similarly, the positive voltage $v_2$ acting alone produces a negative output voltage hence $v_2$ is called inverting input. Consequently $B_1$ is called noninverting input terminal and $B_2$ is called inverting input terminal.

Common mode Gain:

A common mode signal is one that drives both inputs of a differential amplifier equally. The common mode signal is interference, static and other kinds of undesirable pickup etc.

The connecting wires on the input bases act like small antennas. If a differential amplifier is operating in an environment with lot of electromagnetic interference, each base picks up an unwanted interference voltage. If both the transistors were matched in all respects then the balanced output would be theoretically zero. This is the important characteristic of a differential amplifier. It discriminates against common mode input signals. In other words, it refuses to amplify the common mode signals.

The practical effectiveness of rejecting the common signal depends on the degree of matching between the two CE stages forming the differential amplifier. In other words, more closely are the currents in the input transistors, the better is the common mode signal rejection e.g. If $v_1$ and $v_2$ are the two input signals, then the output of a practical op-amp cannot be described by simply
In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).

\[ v_d = (v_1 - v_2) \]

and \[ v_C = \frac{1}{2} (v_1 + v_2) \]

The output voltage, therefore can be expressed as

\[ v_O = A_1 v_1 + A_2 v_2 \]

Where \( A_1 \) & \( A_2 \) are the voltage amplification from input 1(2) to output under the condition that input 2 (1) is grounded.

\[ \therefore v_1 = v_C + \frac{1}{2} v_d \quad v_2 = v_C - \frac{1}{2} v_d \]

Substituting \( v_1 \) & \( v_2 \) in output voltage equation

\[ v_O = A_1 (v_C + \frac{1}{2} v_d) + A_2 (v_C - \frac{1}{2} v_d) \]

\[ = \frac{1}{2} (A_1 - A_2) v_d + (A_1 - A_2) v_C \]

\[ = A_d v_d + A_C v_C \]

The voltage gain for the difference signal is \( A_d \) and for the common mode signal is \( A_C \).

The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio (CMRR). It is the ratio of differential gain \( A_d \) to the common mode gain \( A_C \).

\[ CMRR = \frac{A_d}{A_C} = \rho \]

\[ \therefore v_O = A_d v_d \left(1 + \frac{1}{\rho} \frac{v_C}{v_d}\right) \]

Date sheet always specify CMRR in decibels \( CMRR = 20 \log CMRR \).

Therefore, the differential amplifier should be designed so that \( \rho \) is large compared with the ratio of the common mode signal to the difference signal. If \( \rho = 1000 \), \( v_C = 1 \text{mV} \), \( v_d = 1 \text{mV} \), then

\[ \frac{1}{\rho} \frac{v_C}{v_d} = \frac{1}{1000} \times \frac{1000 \mu V}{1 \mu V} = 1 \]

It is equal to first term. Hence for an amplifier with \( \rho = 1000 \), a 1 mV difference of potential between two inputs gives the same output as 1 mV signal applied with the same polarity to both inputs.
Dual Input, Unbalanced Output Differential Amplifier:

In this case, two input signals are given however the output is measured at only one of the two-collector w.r.t. ground as shown in fig. 2. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground.

![Fig. 2](image)

In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

\[
\begin{align*}
I_E &= I_C0 = \frac{V_{EE} \cdot V_{BE}}{2R_E + \frac{R_2}{\beta_{dc}}} \\
V_{CEO} &= V_{CC} + V_{BE} - I_{C0}R_C
\end{align*}
\]

AC Analysis:

The output voltage gain in this case is given by

\[
A_d = \frac{V_o}{V_d} = \frac{R_C}{2r'_e}
\]

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since at the output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

Differential amplifier with swamping resistors:

By using external resistors $R'_E$ in series with each emitter, the dependence of voltage gain on variations of $r'_e$ can be reduced. It also increases the linearity range of the differential amplifier.
**Fig. 3.** shows the differential amplifier with swamping resistor $R'_E$. The value of $R'_E$ is usually large enough to swamp the effect of $r'_e$.

\[
\begin{align*}
R_1 I_B + V_{BE} + R'_E I_E + 2 R_E I_E &= V_{EE} \\
R_1 I_E / \beta_{dc} + V_{BE} + R'_E I_E + 2 R_E I_E &= V_{EE}
\end{align*}
\]

From the equation, $I_E$ can be obtained as

\[
I_E = \frac{V_{EE} - V_{BE}}{R'_E + 2R_E + R_1 / \beta_{dc}}
\]

\[
V_{CEO} = V_{CC} + V_{BE} - I_C R_C
\]

The new voltage gain is given by $A_d = \frac{V_{CC} - V_{BE}}{R'_E}$

The input resistance is given by $R_{in1} = R_{in2} = 2 \beta_1 (r'_e + R'_E)$

The output resistance with or without $R'_E$ is the same i.e.

\[
R_{o1} = R_{o1} = R_C
\]

**Example-1**

Consider example-1 of lecture-2. The specifications are given again for the dual input, unbalanced-output differential amplifier: $R_C = 2.2 \, k\Omega$, $R_B = 4.7 \, k\Omega$, $R_{in1} = R_{in2} = 50\Omega$, $+V_{CC} = 10\, V$, $-V_{EE} = -10\, V$, $\beta_{dc} = 100$ and $V_{BE} = 0.715\, V$.

Determine the voltage gain, input resistance and the output resistance.

Notes prepared by Mrs. Sejal Shah
Solution:

Since the component values remain unchanged and the biasing arrangement is same, the $I_{CQ}$ and $V_{CEQ}$ values as well as input and output resistance values for the dual input, unbalanced output configuration must be the same as those for the dual input, balanced output configuration.

Thus, $I_{CQ} = 0.988$ mA  
$V_{CEQ} = 8.54$ V  
$R_{i1} = R_{i2} = 5.06$ kΩ  
$R_o = 2.2$ kΩ

The voltage gain of the dual input, unbalanced output differential amplifier is given by

$$A_v = \frac{R_C}{2R_e} = \frac{2.2 \text{ kΩ}}{(2)(25.3)} = 43.8$$

Constant Current Bias:

In the dc analysis of differential amplifier, we have seen that the emitter current $I_E$ depends upon the value of $\frac{\Delta}{dc}$. To make operating point stable $I_E$ current should be constant irrespective value of $\frac{\Delta}{dc}$.

For constant $I_E$, $R_E$ should be very large. This also increases the value of CMRR but if $R_E$ value is increased to very large value, $I_E$ (quiescent operating current) decreases. To maintain same value of $I_E$, the emitter supply $V_{EE}$ must be increased. To get very high value of resistance $R_E$ and constant $I_E$, current, current bias is used.

![Figure 5.1](image-url)
Fig. 1, shows the dual input balanced output differential amplifier using a constant current bias. The resistance $R_E$ is replace by constant current transistor $Q_3$. The dc collector current in $Q_3$ is established by $R_1$, $R_2$, & $R_E$.

Applying the voltage divider rule, the voltage at the base of $Q_3$ is

$$V_{b3} = \frac{R_2}{R_1 + R_2} (V_{EE})$$

$$V_{e3} = V_{b3} \cdot V_{be3}$$

$$= \frac{R_2}{R_1 + R_2} \cdot V_{EE} - V_{be3}$$

$$I_{be3} = I_{C3} = \frac{V_{e3} \cdot (-V_{EE})}{R_E}$$

$$= \frac{V_{EE} \cdot \left(\frac{R_2}{R_1 + R_2}\right)}{R_E} \cdot V_{EE} - V_{be3}$$

Because the two halves of the differential amplifiers are symmetrical, each has half of the current $I_{C3}$.

$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} \cdot \left[\frac{R_2}{R_1 + R_2} \cdot V_{EE}\right]}{2R_E} \cdot V_{be3}$$

The collector current, $I_{C3}$ in transistor $Q_3$ is fixed because no signal is injected into either the emitter or the base of $Q_3$.

Besides supplying constant emitter current, the constant current bias also provides a very high source resistance since the ac equivalent of the dc source is ideally an open circuit. Therefore, all the performance equations obtained for differential amplifier using emitter bias are also valid.

As seen in $I_E$ expressions, the current depends upon $V_{be3}$. If temperature changes, $V_{be}$ changes and current $I_E$ also changes. To improve thermal stability, a diode is placed in series with resistance $R_1$ as shown in Fig. 2.
This helps to hold the current $I_{E3}$ constant even though the temperature changes. Applying KVL to the base circuit of $Q_3$.

\[
(V_{EE} - V_D) \frac{R_1}{R_1 + R_2} + V_D = V_{BE3} + I_{E3} R_E
\]

where $V_D$ is the diode voltage. Thus,

\[
I_{E3} = \frac{1}{R_E} \left\{ V_{EE} \frac{R_1}{R_1 + R_2} + V_D \frac{R_1}{R_1 + R_2} \cdot V_{BE3} \right\}
\]

If $R_1$ and $R_2$ are so chosen that

\[
\frac{R_2}{R_1 + R_2} V_D = V_{BE3}
\]

then,

\[
I_{E3} = \frac{1}{R_3} \cdot \frac{V_{EE} R_1}{R_1 + R_2}
\]

Therefore, the current $I_{E3}$ is constant and independent of temperature because of the added diode D. Without D the current would vary with temperature because $V_{BE3}$ decreases approximately by 2mV/°C. The diode has same temperature dependence and hence the two variations cancel each other and $I_{E3}$ does not vary appreciably with temperature. Since the cut ? in voltage $V_D$ of diode approximately the same value as the base to emitter voltage $V_{BE}$ of a transistor the above condition cannot be satisfied with one diode. Hence two diodes are used in series for $V_D$. In this case the common mode gain reduces to zero.
Some times zener diode may be used in place of diodes and resistance as shown in \textbf{fig. 3}. Zeners are available over a wide range of voltages and can have matching temperature coefficient.

The voltage at the base of transistor Q_B is

\[
V_{B_B} = V_Z - V_{EE} \\
V_{E_E} = V_{B_B} - V_{BE_E} \\
\therefore I_{E_E} = \frac{V_{E_E} \cdot (\cdot V_{EE})}{R_E} \\
= \frac{V_Z - V_{BE_E}}{R_E}
\]

The value of R_2 is selected so that \( I_2 \geq 1.2 I_{Z(min)} \) where \( I_Z \) is the minimum current required to cause the zener diode to conduct in the reverse region, that is to block the rated voltage \( V_Z \).

\[
R_2 = \frac{V_{EE} - V_Z}{I_2}
\]

\textbf{Current Mirror:}

The circuit in which the output current is forced to equal the input current is said to be a current mirror circuit. Thus in a current mirror circuit, the output current is a mirror image of the input current. The current mirror circuit is shown in \textbf{fig. 4}.

Once the current \( I_2 \) is set up, the current \( I_{C3} \) is automatically established to be nearly equal to \( I_2 \). The current mirror is a special case of constant current bias and the current mirror bias requires of constant current bias.
and therefore can be used to set up currents in differential amplifier stages. The current mirror bias requires fewer components than constant current bias circuits.

Since Q3 and Q4 are identical transistors the current and voltage are approximately same

\[ V_{BE3} = V_{BE4} \]
\[ I_{C3} = I_{C4} \]
\[ I_{C3} + 2 I_{C3} = I_{C3} + 2 I_{C3} \]
\[ = I_{C3} \left( 1 + \frac{2}{\beta_{dc}} \right) \]

Generally \( \beta_{dc} \) is large enough, therefore \( \frac{2}{\beta_{dc}} \) is small.

\[ \therefore I_2 \approx I_{C3} \]
\[ I_2 = \frac{V_{EE} + V_{BE0}}{R_2} \]

For satisfactory operation two identical transistors are necessary.

The operation amplifier:

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential (OPAMP) amplifiers and followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package.

The block diagram of OPAMP is shown in fig. 1.

![Fig. 1](image)

The input stage is a dual input balanced output differential amplifier. This stage provides most of the voltage...
gain of the amplifier and also establishes the input resistance of the OPAMP. The intermediate stage of OPAMP is another differential amplifier which is driven by the output of the first stage. This is usually dual input unbalanced output.

Because direct coupling is used, the dc voltage level at the output of intermediate stage is well above ground potential. Therefore level shifting circuit is used to shift the dc level at the output downward to zero with respect to ground. The output stage is generally a push pull complementary amplifier. The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP. It also provides low output resistance.

**Level Translator:**

Because of the direct coupling the dc level at the emitter rises from stage to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

To shift the output dc level to zero, level translator circuits are used. An emitter follower with voltage divider is the simplest form of level translator as shown in fig. 2.

Thus a dc voltage at the base of Q produces 0V dc at the output. It is decided by $R_1$ and $R_2$. Instead of voltage divider emitter follower either with diode current bias or current mirror bias as shown in fig. 3 may be used to get better results.

In this case, level shifter, which is common collector amplifier, shifts the level by 0.7V. If this shift is not sufficient, the output may be taken at the junction of two resistors in the emitter leg.
Fig. 3

**Fig. 4.** shows a complete OPAMP circuit having input different amplifiers with balanced output, intermediate stage with unbalanced output, level shifter and an output amplifier.

![Diagram of a complete OPAMP circuit](image)

**Lecture - 6: Practical Operational Amplifier**

The symbolic diagram of an OPAMP is shown in fig. 1.

![Symbolic diagram of an OPAMP](image)

741c is most commonly used OPAMP available in IC package. It is an 8-pin DIP chip.

**Parameters of OPAMP:**

The various important parameters of OPAMP are follows:

1. Input Offset Voltage:
Operational Amplifier

Notes prepared by Mrs. Sejal Shah

Input offset voltage is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output. Fig. 2, shows that two dc voltages are applied to input terminals to make the output zero.

\[ V_{io} = V_{dc1} - V_{dc2} \]

\( V_{dc1} \) and \( V_{dc2} \) are dc voltages and \( R_S \) represents the source resistance. \( V_{io} \) is the difference of \( V_{dc1} \) and \( V_{dc2} \). It may be positive or negative. For a 741C OPAMP the maximum value of \( V_{io} \) is 6mV. It means a voltage ± 6 mV is required to one of the input to reduce the output offset voltage to zero. The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched.

2. Input offset Current:

The input offset current \( I_{io} \) is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

\[ I_{io} = |IB1 - IB2| \]

The \( I_{io} \) for the 741C is 200nA maximum. As the matching between two input terminals is improved, the difference between \( IB1 \) and \( IB2 \) becomes smaller, i.e. the \( I_{io} \) value decreases further. For a precision OPAMP 741C, \( I_{io} \) is 6 nA

3. Input Bias Current:

The input bias current \( IB \) is the average of the current entering the input terminals of a balanced amplifier i.e.

\[ IB = (IB1 + IB2) / 2 \]

For 741C \( IB(max) = 700 \text{ nA} \) and for precision 741C \( IB = \pm 7 \text{ nA} \)

4. Differential Input Resistance: \( (R_i) \)

\( R_i \) is the equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal grounded. For the 741C the input resistance is relatively high 2 MΩ. For some OPAMP it may be up to 1000 G ohm.

5. Input Capacitance: \( (C_i) \)
Ci is the equivalent capacitance that can be measured at either the inverting and noninverting terminal with the other terminal connected to ground. A typical value of Ci is 1.4 pf for the 741C.

6. Offset Voltage Adjustment Range:

741 OPAMP have offset voltage null capability. Pins 1 and 5 are marked offset null for this purpose. It can be done by connecting 10 K ohm pot between 1 and 5 as shown in fig. 3.

![Fig. 3](image)

By varying the potentiometer, output offset voltage (with inputs grounded) can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying 10 K pot. For the 741C the offset voltage adjustment range is ± 15 mV.

Parameters of OPAMP:

7. Input Voltage Range :

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and noninverting input terminals. For the 741C, the range of the input common mode voltage is ± 13V maximum. This means that the common mode voltage applied at both input terminals can be as high as +13V or as low as -13V.


CMRR is defined as the ratio of the differential voltage gain $A_d$ to the common mode voltage gain $A_{CM}$

$$\text{CMRR} = \frac{A_d}{A_{CM}}.$$  

For the 741C, CMRR is 90 dB typically. The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.
9. Supply voltage Rejection Ratio: (SVRR)

SVRR is the ratio of the change in the input offset voltage to the corresponding change in power supply voltages. This is expressed in V/V or in decibels, SVRR can be defined as

\[ SVRR = \frac{\Delta V_{io}}{\Delta V} \]

Where \( \Delta V \) is the change in the input supply voltage and \( \Delta V_{io} \) is the corresponding change in the offset voltage.

For the 741C, SVRR = 150 µ V / V.

For 741C, SVRR is measured for both supply magnitudes increasing or decreasing simultaneously, with \( R_3 \) = 10K. For same OPAMPS, SVRR is separately specified as positive SVRR and negative SVRR.

10. Large Signal Voltage Gain:

Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as

\[ \text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}} \]
\[ A = \frac{V_o}{V_{iq}} \]

Because output signal amplitude is much large than the input signal the voltage gain is commonly called large signal voltage gain. For 741C is voltage gain is 200,000 typically.

11. Output voltage Swing:

The ac output compliance PP is the maximum unclipped peak to peak output voltage that an OPAMP can produce. Since the quiescent output is ideally zero, the ac output voltage can swing positive or negative. This also indicates the values of positive and negative saturation voltages of the OPAMP. The output voltage never exceeds these limits for a given supply voltages \( +V_{CC} \) and \( -V_{EE} \). For a 741C it is ± 13 V.

12. Output Resistance: (R_O)

\( R_O \) is the equivalent resistance that can be measured between the output terminal of the OPAMP and the ground. It is 75 ohm for the 741C OPAMP.

Example - 1

Determine the output voltage in each of the following cases for the open loop differential amplifier of fig. 4:

a. \( v_{in\ 1} = 5 \text{ m V} \text{ dc}, \ v_{in\ 2} = -7 \mu \text{V dc} \)

b. \( v_{in\ 1} = 10 \text{ mV rms}, \ v_{in\ 2} = 20 \text{ mV rms} \)
Fig. 4

Specifications of the OPAMP are given below:
A = 200,000, R_i = 2 MΩ, R_O = 75Ω, + V_C = + 15 V, - V_EE = - 15 V, and output voltage swing = ± 14V.

Solution:

(a). The output voltage of an OPAMP is given by

\[ v_o = A_d (v_{in1} - v_{in2}) \]
\[ v_o = 200,000 \left( (5) \times 10^{-6} - (-7) \times 10^{-6} \right) = 2.4 \text{ V dc} \]

Remember that \( v_o = 2.4 \text{ V dc} \) with the assumption that the dc output voltage is zero when the input signals are zero.

(b). The output voltage equation is valid for both ac and dc input signals. The output voltage is given by

\[ V_o = 200,000 \left( (10) \times 10^{-3} - (20) \times 10^{-3} \right) = -2000 \text{ V rms} \]

Thus the theoretical value of output voltage \( v_o = -2000 \text{ V rms} \). However, the OPAMP saturates at ± 14 V. Therefore, the actual output waveform will be clipped as shown in fig. 5. This non-sinusoidal waveform is unacceptable in amplifier applications.
13. Output Short circuit Current:

In some applications, an OPAMP may drive a load resistance that is approximately zero. Even its output impedance is 75 ohm but cannot supply large currents. Since OPAMP is low power device and so its output current is limited. The 741C can supply a maximum short circuit output current of only 25mA.

14. Supply Current:

$I_S$ is the current drawn by the OPAMP from the supply. For the 741C OPAMP the supply current is 2.8 mA.

15. Power Consumption:

Power consumption (PC) is the amount of quiescent power ($v_{in}=0V$) that must be consumed by the OPAMP in order to operate properly. The amount of power consumed by the 741C is 85 mW.

16. Gain Bandwidth Product:

The gain bandwidth product is the bandwidth of the OPAMP when the open loop voltage gain is reduced to 1. From open loop gain vs frequency graph At 1 MHz shown in Fig. 6. It can be found 1 MHz for the 741C OPAMP frequency the gain reduces to 1. The mid band voltage gain is 100,000 and cut off frequency is 10Hz.
17. Slew Rate:

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts / µs.

$$SR = \left. \frac{dV_o}{dt} \right|_{max} \frac{V}{\mu s}$$

To understand this, consider a charging current of a capacitor shown in fig. 7.

$$i = C \frac{dV}{dt}$$

$$\frac{dV}{dt} = \frac{i}{C}$$

If 'i' is more, capacitor charges quickly. If 'i' is limited to $I_{max}$, then rate of change is also limited.
Slew rate indicates how rapidly the output of an OPAMP can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain and is normally specified at unity gain.

If the slope requirement is greater than the slew rate, then distortion occurs. For the 741C the slew rate is low 0.5 V / μs, which limits its use in higher frequency applications.

### 18. Input Offset Voltage and Current Drift:

It is also called average temperature coefficient of input offset voltage or input offset current. The input offset voltage drift is the ratio of the change in input offset voltage to change in temperature and expressed in V/°C. Input offset voltage drift = (V_{io}/T).

Similarly, input offset current drift is the ratio of the change in input offset current to the change in temperature. Input offset current drift = (I_{io}/T).

For 741C,

- V_{io}/T = 0.5 V/°C.
- I_{io}/T = 12 pA/°C.

#### Example - 2

An operational amplifier has a slew rate of 2 V/μs. If the peak output is 12 V, what is the power bandwidth?

**Solution:**

The slew rate of an operational amplifier is

\[
SR = 2 \pi f \sqrt{V_p}
\]

\[
f = \frac{SR}{2 \pi \sqrt{V_p}}
\]

As for output free of distortion, the slews determines the maximum frequency of operation f_{max} for a desired output swing.

\[
f_{max} = \frac{1}{2 \pi x 10^{-6}} = 26.5 \text{ kHz}
\]

So bandwidth = 26.5 kHz.

#### Example - 3

For the given circuit in fig. 1, I_{in(off)} = 20 nA. If V_{in(off)} = 0, what is the differential input voltage? If A = 10^5, what does the output offset voltage equal?
Solutin:

\[ I_{\text{in(off)}} = 20 \text{ nA} \]
\[ V_{\text{in(off)}} = 0 \]

(i) The differential input voltage = \( I_{\text{in(off)}} \times 1k = 20 \text{ nA} \times 1k = 20 \mu \text{ V} \)

(ii) If \( A = 10^5 \) then the output offset voltage \( V_{\text{in(off)}} = 20 \mu \text{ V} \times 10^5 = 2 \text{ volt} \)

Output offset voltage = 2 volts.

Open loop OPAMP Configuration:

In the case of amplifiers the term open loop indicates that no connection, exists between input and output terminals of any type. That is, the output signal is not feedback in any form as part of the input signal.

In open loop configuration, The OPAMP functions as a high gain amplifier. There are three open loop OPAMP configurations.

The Differential Amplifier:

**Fig. 1.** shows the open loop differential amplifier in which input signals \( v_{\text{in1}} \) and \( v_{\text{in2}} \) are applied to the positive and negative input terminals.
Fig. 1

Since the OPAMP amplifies the difference between the two input signals, this configuration is called the differential amplifier. The OPAMP amplifies both ac and dc input signals. The source resistance $R_{in1}$ and $R_{in2}$ are normally negligible compared to the input resistance $R_i$. Therefore voltage drop across these resistances can be assumed to be zero.

Therefore

$$v_1 = v_{in1} \text{ and } v_2 = v_{in2}.$$  

$$v_o = A_d (v_{in1} - v_{in2})$$

where, $A_d$ is the open loop gain.

**The Inverting Amplifier:**

If the input is applied to only inverting terminal and non-inverting terminal is grounded then it is called inverting amplifier. This configuration is shown in fig. 2:

$$v_1 = 0, \ v_2 = v_{in}.$$  

$$v_o = -A_d \ v_{in}$$
Operational Amplifier

The negative sign indicates that the output voltage is out of phase with respect to input 180° or is of opposite polarity. Thus the input signal is amplified and inverted also.

**The non-inverting amplifier:**

In this configuration, the input voltage is applied to non-inverting terminals and inverting terminal is ground as shown in fig. 3.

\[ v_1 = +v_{\text{in}} \quad v_2 = 0 \]

\[ v_o = +A_{d} v_{\text{in}} \]

This means that the input voltage is amplified by \( A_{d} \) and there is no phase reversal at the output.

In all the configurations any input signal slightly greater than zero drive the output to saturation level. This is because of very high gain. Thus when operated in open-loop, the output of the OPAMP is either negative or positive saturation or switches between positive and negative saturation levels. Therefore open loop op-amp is not used in linear applications.
Closed Loop Amplifier:

The gain of the OPAMP can be controlled if feedback is introduced in the circuit. That is, an output signal is feedback to the input either directly or via another network. If the signal feedback is of opposite or out phase by 180° with respect to the input signal, the feedback is called negative feedback.

An amplifier with negative feedback has a self-correcting ability of change in output voltage caused by changes in environmental conditions. It is also known as degenerative feedback because it reduces the output voltage and, in turn, reduces the voltage gain.

If the signal is feedback in phase with the input signal, the feedback is called positive feedback. In positive feedback the feedback signal aids the input signal. It is also known as regenerative feedback. Positive feedback is necessary in oscillator circuits.

The negative feedback stabilizes the gain, increases the bandwidth and changes, the input and output resistances. Other benefits are reduced distortion and reduced offset output voltage. It also reduces the effect of temperature and supply voltage variation on the output of an op-amp.

A closed loop amplifier can be represented by two blocks one for an OPAMP and other for a feedback circuits. There are four following ways to connect these blocks. These connections are shown in fig. 4.

These connections are classified according to whether the voltage or current is feedback to the input in series or in parallel:

- Voltage ? series feedback
- Voltage ? shunt feedback
- Current ? series feedback
- Current ? shunt feedback
In all these circuits of Fig. 4, the signal direction is from input to output for OPAMP and output to input for feedback circuit. Only first two, feedback in circuits are important.

Voltage series feedback:

It is also called non-inverting voltage feedback circuit. With this type of feedback, the input signal drives the non-inverting input of an amplifier; a fraction of the output voltage is then fed back to the inverting input. The op-amp is represented by its symbol including its large signal voltage gain $A_d$ or $A$, and the feedback circuit is composed of two resistors $R_1$ and $R_f$ as shown in Fig. 5.
Operational Amplifier

Open loop voltage gain $A_d = \frac{V_o}{V_d}$

Closed loop voltage gain $A_{CL} = \frac{V_o}{V_{in}}$

Feedback circuit gain $B = \frac{V_i}{V_o}$

The differential voltage input $V_d = V_{in} - V_f$

The feedback voltage always opposes the input voltage, (or is out of phase by 180° with respect to input voltage), hence the feedback is said to be negative.

The closed loop voltage gain is given by

$$A_{CL} = \frac{V_o}{V_{in}}$$

$$V_o = A (V_i - V_f) = A (V_{in} - V_f) = A (V_{in} - BV_o)$$

$$V_o (1 + AB) = A V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{A}{1 + AB}$$

The product $A$ and $B$ is called loop gain. The gain loop gain is very large such that $AB >> 1$

$$\therefore \frac{V_o}{V_{in}} = \frac{A}{AB} = \frac{1}{B}$$

$$= \frac{R_1 + R_f}{R_1}$$

$$= 1 + \frac{R_f}{R_1}$$

This shows that overall voltage gain of the circuit equals the reciprocal of $B$, the feedback gain. It means that closed loop gain is no longer dependent on the gain of the op-amp, but depends on the feedback of the voltage divider. The feedback gain $B$ can be precisely controlled and it is independent of the amplifier.

Physically, what is happening in the circuit? The gain is approximately constant, even though differential voltage gain may change. Suppose $A$ increases for some reasons (temperature change). Then the output voltage will try to increase. This means that more voltage is feedback to the inverting input, causing $V_d$ voltage to decrease. This almost completely offset the attempted increases in output voltage.

Similarly, if $A$ decreases, The output voltage decreases. It reduces the feedback voltage $V_f$ and hence, $V_d$ voltage increases. Thus the output voltage increases almost to same level.

Notes prepared by Mrs. Sejal Shah
Different Input voltage is ideally zero.

Again considering the voltage equation,

\[ v_O = A_d \cdot v_d \]

or \[ v_d = v_O / A_d \]

Since \( A_d \) is very large (ideally infinite)

\[ v_d = 0. \]

and \[ v_1 = v_2 \] (ideal).

This says, that the voltage at non-inverting input terminal of an op-amp is approximately equal to that at the inverting input terminal provided that \( A_d \) is very large. This concept is useful in the analysis of closed loop OPAMP circuits. For example, ideal closed loop voltage again can be obtained using the results

\[
\begin{align*}
v_1 &= v_{in} \\
v_2 &= v_I = \frac{R_1}{R_1 + R_f} v_o \\
\therefore v_1 &= v_2 \\
\therefore v_{in} &= \frac{R_1}{R_1 + R_f} v_o \\
v_o &= \left(1 + \frac{R_1}{R_f}\right) v_{in}
\end{align*}
\]

Input Resistance with Feedback:

**fig. 1.** shows a voltage series feedback with the OPAMP equivalent circuit.
In this circuit $R_i$ is the input resistance (open loop) of the OPAMP and $R_{if}$ is the input resistance of the feedback amplifier. The input resistance with feedback is defined as

$$R_{if} = \frac{v_{in}}{i_{in}}$$
$$v_{in} = v_d + v_f$$
$$= v_d + BV_o$$
$$= v_d + BA v_d$$
$$= v_d (1 + AB)$$
$$= (1 + AB) i_{in} R_i$$

Thus, $R_{if}$ approaches infinity and therefore, this amplifier approximates an ideal voltage amplifier.

**Output Resistance with Feedback:**

Output resistance is the resistance determined looking back into the feedback amplifier from the output terminal. To find output resistance with feedback $R_f$, input $v_{in}$ is reduced to zero, an external voltage $V_o$ is applied as shown in **fig. 2**.
The output resistance ($R_{of}$) is defined as:

$$R_{of} = \frac{V_{in}}{i_{in}}$$

$$i = i_a + i_b$$

since \(\left(\frac{R_1 R_2}{2} + R_f\right) \gg R_o\)

\(i \approx i_a\)

Applying KVL output loop

\(v = v_o - v_{12} = 0 - Bv\)

\(v_d = v_{12}\)

\(i = \frac{v - A_v v_o}{R_o} = \frac{v - A_B v_o}{R_o}\)

\(R_{of} = \frac{v}{i_o} = \frac{R_o}{1+AB}\)

This shows that the output resistance of the voltage series feedback amplifier is \((1 / 1+AB)\) times the output resistance $R_o$ of the op-amp. It is very small because $(1+AB)$ is very large. It approaches to zero for an ideal voltage amplifier.

**Bandwidth with Feedback:**

The bandwidth of an amplifier is defined as the band of frequencies for which the gain remains constant. **Fig. 3** shows the open loop gain vs frequency curve of 741C OPAMP. From this curve for a gain of $2 \times 10^5$ the
bandwidth is approximately 5Hz. On the other hand, the bandwidth is approximately 1MHz when the gain is unity.

![Graph showing frequency vs gain for an operational amplifier](image)

**Fig. 3**

The frequency at which gain equals 1 is known as the unity gain bandwidth. It is the maximum frequency the OPAMP can be used for.

Furthermore, the gain bandwidth product obtained from the open loop gain vs frequency curve is equal to the unity gain bandwidth of the OPAMP.

Since the gain bandwidth product is constant obviously the higher the gain the smaller the bandwidth and vice versa. If negative feedback is used gain decrease from A to A / (1+AB). Therefore the closed loop bandwidth increases by (1+AB).

\[
\text{Bandwidth with feedback} = (1 + A \cdot B) \times (\text{B.W. without feedback})
\]

\[
f_f = f_0 (1 + A \cdot B)
\]

**Output Offset Voltage:**

Notes prepared by Mrs. Sejal Shah
In an OPAMP even if the input voltage is zero an output voltage can exist. There are three cause of this unwanted offset voltage.

1. Input offset voltage.
2. Input bias voltage.
3. Input offset current.

**Fig. 4** shows a feedback amplifier with an output offset voltage source in series with the open loop output $AV_d$. The actual output offset voltage with negative feedback is smaller. The reasoning is similar to that given for distortion. Some of the output offset voltage is fed back to the inverting input. After amplification an out of phase voltage arrives at the output canceling most of the original output offset voltage.

$$\text{Total output offset voltage with feedback} = \frac{V_{out(0)}}{1+AB}$$

When loop gain $AB$ is much greater than 1, the closed loop output offset voltage is much smaller than the open loop output offset voltage.

**Voltage Follower:**

The lowest gain that can be obtained from a non-inverting amplifier with feedback is 1. When the non-inverting amplifier gives unity gain, it is called voltage follower because the output voltage is equal to the input voltage and in phase with the input voltage. In other words the output voltage follows the input voltage.

To obtain voltage follower, $R_1$ is open circuited and $R_f$ is shorted in a negative feedback amplifier of **fig. 4**. The resultant circuit is shown in **fig. 5**.

$$v_{out} = Av_d = A (v_1 - v_2)$$

$$v_1 = v_{in}$$

$$v_2 = v_{out}$$

$$v_1 = v_2 \text{ if } A \gg 1$$

$$v_{out} = v_{in}$$

The gain of the feedback circuit (B) is 1.
Therefore

\[ A_f = \frac{1}{B} = 1 \]

**Voltage shunt Feedback:**

Fig. 1, shows the voltage shunt feedback amplifier using OPAMP.

The input voltage drives the inverting terminal, and the amplified as well as inverted output signal is also applied to the inverting input via the feedback resistor \( R_f \). This arrangement forms a negative feedback because any increase in the output signal results in a feedback signal into the inverting input signal causing a decrease in the output signal. The non-inverting terminal is grounded. Resistor \( R_1 \) is connected in series with the source.

The closed loop voltage gain can be obtained by, writing Kirchoff's current equation at the input node \( V_2 \).
Operational Amplifier

The negative sign in equation indicates that the input and output signals are out of phase by 180. Therefore it is called inverting amplifier. The gain can be selected by selecting \( R_f \) and \( R_1 \) (even < 1).

**Inverting Input at Virtual Ground:**

In the fig. 1, shown earlier, the noninverting terminal is grounded and the input signal is applied to the inverting terminal via resistor \( R_1 \). The difference input voltage \( v_d \) is ideally zero, \( (v_d = \frac{v_o}{A}) \) is the voltage at the inverting terminals \( (v_2) \) is approximately equal to that of the noninverting terminal \( (v_1) \). In other words, the inverting terminal voltage \( (v_1) \) is approximately at ground potential. Therefore, it is said to be at virtual ground.

\[
\begin{align*}
\frac{i_n}{R_1} & \approx i_f \\
\frac{v_{in} - v_2}{R_1} & = \frac{v_2 - v_o}{R_f} \\
v_1 & = v_2 = 0V \\
v_{in} & = \frac{-v_o}{R_1} \\
v_o & = -\frac{R_f}{R_1}v_{in}
\end{align*}
\]

**Input Resistance with Feedback:**

The negative sign in equation indicates that the input and output signals are out of phase by 180. Therefore it is called inverting amplifier. The gain can be selected by selecting \( R_f \) and \( R_1 \) (even < 1).
To find the input resistance Miller equivalent of the feedback resistor $R_f$, is obtained, i.e. $R_f$ is split into its two Miller components as shown in fig. 2. Therefore, input resistance with feedback $R_{if}$ is then

$$R_{if} = R_i + \left( \frac{R_f}{1+A} \right)$$

Since $R_i$ and $A$ are very large, therefore,

$$\left( \frac{R_f}{1+A} \right) \approx 0 \text{ ohm}$$

Hence $R_{if} = R_i$

**Output Resistance with Feedback:**

The output resistance with feedback $R_{of}$ is the resistance measured at the output terminal of the feedback amplifier. The output resistance can be obtained using Thevenin’s equivalent circuit, shown in fig. 3.

$$i_O = i_a + i_b$$

Since $R_o$ is very small as compared to $R_f + (R_1 \parallel R_2)$

Therefore, i.e. $i_O = i_a$

$$v_O = R_o i_O + A v_d$$

$$v_d = v_1 - v_2 = 0 - B v_O$$

$$i_O = \frac{v_o - A v_d}{R_o}$$

$$= \frac{v_0 - A B v_o}{R_0}$$

$$R_{or} = \frac{v_o}{i_O} = \frac{R_0}{1 + AB}$$

where, $B = \frac{R_1}{R_f}$

Similarly, the bandwidth increases by $(1+AB)$ and total output offset voltage reduces by $(1+AB)$. 

Notes prepared by Mrs. Sejal Shah