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# CONTENTS

**Volume 4**  
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<table>
<thead>
<tr>
<th>S. No</th>
<th>Title</th>
<th>Authors</th>
<th>Page No</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.</td>
<td>Control of DC Voltage in Multi-Terminal VSC HVDC Systems with Fuzzy Logic Controller</td>
<td>Harika and G.Anil</td>
<td>11</td>
</tr>
<tr>
<td>3.</td>
<td>Improve Efficiency on Grid Feeding Current Source Inverter for Solar Photovoltaic System</td>
<td>Mirala Yamuna and HabeebFathima</td>
<td>22</td>
</tr>
<tr>
<td>4.</td>
<td>Improvement of Transient Response of DSTATCOM Using Fast Acting DC Link Voltage Controller</td>
<td>Md Sartaz Baba, Anumandla Swetha</td>
<td>33</td>
</tr>
<tr>
<td>5.</td>
<td>Multilevel Converters Based on VSC on Railway Electrification System</td>
<td>J.Navya, M.Lakpathi and P.Baburao</td>
<td>42</td>
</tr>
<tr>
<td>6.</td>
<td>Speed Control of BLDC Motor Drive by Using Buck-Boost Converter</td>
<td>Maisakshi.Pavan Kumar and J.Devender</td>
<td>52</td>
</tr>
<tr>
<td>7.</td>
<td>Designing of Data Matching Encoded System Low Complexity Using BWA</td>
<td>Naresh Chilpuri</td>
<td>59</td>
</tr>
<tr>
<td>8.</td>
<td>Designing of Fast Multiplication System for RNS (Cryptography)</td>
<td>S.Laxminarayana</td>
<td>64</td>
</tr>
<tr>
<td>9.</td>
<td>Designing of Multi Band Clock Distribution for SOC/NOC Application</td>
<td>Sushma Anchuri and Tharuni.M</td>
<td>71</td>
</tr>
<tr>
<td>No.</td>
<td>Title</td>
<td>Authors</td>
<td>Page</td>
</tr>
<tr>
<td>------</td>
<td>----------------------------------------------------------------------</td>
<td>----------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>10.</td>
<td>Designing of Self Timed Adder by Using CMOS Technology</td>
<td>Doobala Naresh and Srujana M</td>
<td>78</td>
</tr>
<tr>
<td>11.</td>
<td>GSM Based Automatic Energy Meter Reading System with Instant Billing</td>
<td>Goli Srivani and V Ramakrishna Reddy</td>
<td>84</td>
</tr>
<tr>
<td>12.</td>
<td>Designing of Integer DCT Architectures for HEVC</td>
<td>Matla Madhavi and M. Tharuni</td>
<td>90</td>
</tr>
<tr>
<td>13.</td>
<td>Built-in Generation of Functional Broadside Tests for Multiple Hard Ware Block on SOC System</td>
<td>Kasthuri Kavitha and M.Srujana</td>
<td>96</td>
</tr>
<tr>
<td>14.</td>
<td>Designing and Comparative Analyses of Carry Select Adders (CSL, CSL with BEC, CSL with CBL)</td>
<td>Shanigarapu Chaithanya and M.Srujana</td>
<td>101</td>
</tr>
<tr>
<td>15.</td>
<td>Design of Digit-Serial FIR Filters Using Shifting and Adding Method</td>
<td>Moutam Komala and M.Srujana</td>
<td>106</td>
</tr>
<tr>
<td>16.</td>
<td>Designing of Fast Decimal Multiplication System by Using BCD Codes</td>
<td>Mothukuri Nagaraju and Mysa Tharuni</td>
<td>110</td>
</tr>
<tr>
<td>17.</td>
<td>Improve Unbalanced Dc Sources by Using Natural Voltage Modulation in Multilevel Inverters</td>
<td>V.Likitha, SK Fathima and K. Sravanthi</td>
<td>116</td>
</tr>
<tr>
<td>18.</td>
<td>An Anti-Islanding Protection of Distributed Generation with Fuzzy Logic Controller</td>
<td>S. Shyamala and S. Ranjith Kumar</td>
<td>127</td>
</tr>
<tr>
<td>19.</td>
<td>Control of a Hybrid Multilevel Converter with Floating DC-links for Current Waveform Improvement</td>
<td>P. Sireesha, Shahima Sherien and K. Sravanthi</td>
<td>136</td>
</tr>
<tr>
<td>20.</td>
<td>Improve Dynamic Response for Fault Current Characteristics of The DFIG with Fuzzy Logic Controller</td>
<td>V. Aruna Kumari and Shahima Sherien</td>
<td>142</td>
</tr>
<tr>
<td></td>
<td>Title</td>
<td>Pages</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>----------------------------------------------------------------------</td>
<td>-------</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Sootrapu Ravi, Shahima Sherien and K.Sravanthi</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22.</td>
<td>Photovoltaic Power Generation System with Five Level Inverter</td>
<td>164</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>K.Ashwini and M.Satyanarayana</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23.</td>
<td>Space Vector Pulse Width Amplitude Modulation for a Buck-Boost Voltage Source Five Level Inverter</td>
<td>178</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>B.Swathi, Sk.Fathima and K.Sravanthi</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24.</td>
<td>SRAM Cells Using Test Vector Monitoring in BIST Architecture for SOC</td>
<td>190</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>S.Mallesh and M.Srujana</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Editorial......

You will be happy to know that we have entered the fourth year of publication of IJ MER, since its inception in April 2012. Focusing on many interdisciplinary subjects, the published papers are spreading the knowledge with fervent hope of upholding the holistic approach. With all my heart, I reiterate to echo my sincere feelings and express my profound thanks to each and every valued contributor. This journal continues to nurture and enhance the capabilities of one and all associated with it.

We as a team with relentless efforts are committed to inspire the readers and achieve further progress. Aim is to sustain the tempo and improve. We acknowledge with pleasure that our readers are enjoying the publications of Sucharita Publishers. We solicit to receive ideas and comments for future improvements in its content and quality. Editor-in-Chief explicitly conveys his gratitude to all the Editorial Board members. Your support is our motivation. Best wishes to everyone.

Dr. K. Victor Babu
Editor-in-Chief
Circuit Breaker Testing ON Single-Phase AC-AC Converter

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Abstract: This paper presents a new novel single-phase ac-ac converter having power factor static correction and output recent control for circuit-breaker testing good IEC 60898 typical. The important aspects of the proposed world are low aspect count and fast responses for the standard requirement, especially a current step at the start of the examination. The proposed single-phase ac-ac converter could operate in either buck or boost mode to match the need for numerous output current although satisfying the ramping along with step current requirements within the standard. The control circuits include things like two parts, dc voltage manage of dc-link capacitors along with ac output recent controls operating concurrently. The proposed world is verified as a result of both computer simulation along with hardware experiment. Certainly one of a 50A world breaker testing good IEC 60898 is demonstrated within the paper.

1 Introduction

A circuit-breaker (CB) is indispensable equipment in residential, commercial and industrial systems. It is designed to protect an electrical circuit from damage caused by overload or short circuit. The capability of interrupting the flow of the current to protect devices enables its utilization in virtually every applications. The time tripping characteristics of the CB and the test procedures detailed in IEC 60898 are necessary in the process of quality control. Commercially available current sources for CB testing are designed using a motor-driven tap-changing auto-transformer for ac output current regulation. Recently, several ac-ac converters have been developed and improved in terms of higher current rating capability and higher efficiency. Also, they have included the power factor correction (PFC) to regulate the input current to be sinusoidal wave shaping with nearly unity power factor. In practice, the ac-ac converters are widely applied to various industrial applications such as UPS, voltage stabilizer, electric welding, and etc.

Several topologies of single-phase ac-ac converter had been reported. The single-phase ac-ac two-leg, three-leg and fourleg (two full-bridges) converters have been presents. They are widely adopted choices of converters in UPS, motor drive or grid-connected applications. These topologies consist mainly of two stages; a controlled rectifier (e.g., boost PFC topology) and a single-phase inverter. They can be operated in either buck or boost mode for the desired level of ac output voltage. The output frequency is controllable and can be set to the values different from the input frequency. The three-leg and two-leg single-phase ac-ac converters are operated in hard switching scheme, producing the switching loss and electromagnetic interferences. In addition, the two-leg single-phase converter has high ripple voltage at the
dc-link capacitors. In a buck-type ac-ac converter reported in, the ac output voltage is controlled using the modified sinusoidal pulsed-width modulation (SPWM).

The single-phase ac-ac converter has been presented in the system application for CB testing according to the CB testing standard (IEC 60898) in Table I. It used four switches to control input current and output current with the same ground. The first part integrates rectifier and boost converter to regulate the dc-link voltages and control the ac input current with sinusoidal waveform in phase with the ac input voltage. The output current control is based on half-bridge topology to drive the positive and negative pulses by means of SPWM technique to the output. Recently, a novel single phase ac-ac converter has been presented and it is also suitable for CB testing application because it supports all key requirements of CB testing standard. This converter operates similarly with converter in, but its difference is about the converter output separated ground instead of shared ground. The ac-ac converter application for CB testing does not require the ac current output sharing the same ground with ac input voltage. As a result, the novel ac-ac converter has been selected to implement the proposed system for CB testing application.

2. Proposed System

The proposed system is shown in Fig. 2.1. The ac-ac converter topology consists of four main switches (1 S - 4 S), two dc-link capacitors (1 C and 2 C), an inductor (s L), diodes (1 D - 6 D), and a power transformer (T1). In the system, the C1 V, C2 V, s i and s v are measured and fed back to the digital controller. The dc-link capacitor (1 C) is charged and C1 V is maintained constant during the positive cycle of s v while the capacitor voltage C2 V is charged and maintained constant during the negative cycle. The input voltage is used as the reference signal for controlling the input current, s i. The output current is regulated by the switches 1 S and 3 S during the positive pulse while the switches 2 S and 4 S operate during the negative pulse, using the sinusoidal PWM (SPWM) technique. The primary winding of the power transformer 1 T, with a turn ratio of 86.3, is connected to the output of the dc-ac converter. The transformer’s secondary winding is short-circuited through the CB during testing. The output current is amplified by an order of the 1 T’s turn ratio. The proposed topology yields power factor in the range of (0.97-0.99) under various output frequencies.

Fig. 2.1. Proposed ac-ac converter with dc-link voltage and ac output current controllers.

3. Integrated Rectifier/Boost Converter

The integrated rectifier and boost converter in the proposed system include three functions as follows. 

a) Rectifying the input voltage into a dc voltage signal;
b) Boosting the dc voltage;
c) Shaping the ac input current to be sinusoidal waveform.

The switches 1 S and 2 S are operated during the positive half cycle.
of the input voltage $v$ to boost the voltage of the dc-link capacitor $C_1$. The waveform of the input voltage $v$ is used as a reference for shaping the inductor current ($i$). The aim is to force the input current $i$ to be in phase with the input voltage for unity power factor. Meanwhile, the capacitor voltage, $C_1V$, is maintained to a constant value. Figs. 1.2 and 1.3 show the circuit configurations during the charging and discharging cycles of the inductor current $i$. During the positive cycle of the input voltage, the switches 1S and 2S are turned on and the inductor current $i$ increases as shown in Fig. 3.1(a). To complete the boost cycle, the switch 1S or 2S is turned off, depending on the output pulses, and the inductor current $i$ is decreased, as shown in Fig. 3.1(b). Similarly, the operations of charging and discharging inductor current during the negative half cycle of the input voltage are repeated through switches 3S and 4S, as shown in Fig. 3.2.

4. DC-AC converter
The proposed dc-ac converter is described in this section. The switches 1S and 3S are turned on to drive positive pulses to the converter output from the dc-link voltage, $C_1V$, as shown in Fig. 1.4(a). Similarly, during the negative output pulse, the dc-link voltage $C_2V$ is connected to the converter output by turning on the switches 2S and 4S, as shown in Fig. 1.4(b). The output of the dc-ac converter is directly connected to the primary winding of the transformer $T$. The transformer’s secondary winding is short-circuited through the CB under test. At this stage, the transformer leakage reactance and resistance form a low-pass filter path for the converter’s output signal. With a proper selection of the switching frequency, a low distortion sinusoidal current at the transformer secondary can be obtained. The output voltage is

$$V_o = \frac{m_a}{\sqrt{2}} \cdot V_{Cl}$$

where $m_a$ is the amplitude modulation index and $ClV$ is the dc-link capacitor voltage.
Fig. 4.1. Circuit configurations under a) positive and c) negative pulses of bipolar SPWM operation, b) and d) commutation current.

4.1 Power Transformer

Since the current required for the CB testing is in the range of hundreds of amperes, a transformer is included in the proposed system. The addition of the transformer serves two purposes, a low-pass filter circuitry and a current amplification for the desired output current. Taking the transformer’s impedance into consideration, the cutoff frequency ($f_c$) of the low-pass filter circuit is given as

$$f_c = \frac{R_{eq}}{2\pi L_{eq}}$$

where $eq X$ and $eq R$ are the equivalent leakage reactance and resistance of the transformer, respectively. The important benefit of the current amplification capability enables the use of low current rating switching devices in the converter. Even though the converter supplies a bipolar SPWM signal to the transformer, the majority of the transformer’s current is the line frequency component therefore, an iron core transformer is chosen. Note that during the CB testing, once the tripping mechanism is initiated, the current through the circuit breaker becomes zero indicating that the secondary of the transformer is open. However, there is a small amount of current supplying the transformer under no-load condition. The proposed system has been designed the turn ratio of 86 for power transformer, using as the current gain amplifier. The output current is controlled by feeding primary side current back into controller for current regulation.

4.2 Controller

The controls of the proposed system are divided into two parts. The first part is the ac input current control for PFC and the dc-link capacitor voltage control. The block diagram of the first part is shown in Fig.4.2. The reference signal is obtained from the input voltage for shaping the input current. Each dc-link capacitor voltage is measured and fed through a PI controller. The outputs of two PI controllers are toggling alternately with the cycle of input voltage. The absolute ac input voltage is multiplied by the output of multiplex block to generate a reference signal for the input current. Next, the error of the input current is sent to a PID controller. The output of the PID controller is then modulated with a triangular signal to generate a PWM signal for the PFC part.

![Fig. 4.2. Block diagram for PFC current control.](image1)

The second part is the output current control illustrated in Fig.4.3. The PID controller is used as a control signal to create PWM signals for the switches $1 \, S_1, \, 2 \, S_2, \, 3 \, S_3$ and $4 \, S_4$, in Fig.1.1. The output of dc-ac converter is connected to the primary winding of the transformer $1 \, T$. Note that the current
control is through the transformer’s primary current. This means that the current transformation ratio must be known a priori to properly compensate for the secondary current control. In the mixing gate control signals block, there are two mixing controls, SPWM signals and PFC signal for ac input current control. The mixing of gate control signals can be logically expressed as follows,

\[
S_1 = \text{SPWM \ OR \ (PFC \ AND \ Cycle)} \ \\
S_2 = \frac{\text{SPWM \ OR \ (PFC \ AND \ Cycle)}}{2} \ \\
S_3 = \text{SPWM \ OR \ (PFC \ AND \ Cycle)} \ \\
S_4 = \frac{\text{SPWM \ OR \ (PFC \ AND \ Cycle)}}{4}
\]

where SPWM is a digital logic signal created by the SPWM switching scheme, PFC is a digital logic signal of the input current control and Cycle is a digital logic signal representing the positive cycle of the input voltage. The switches 1 \( S \) and 3 \( S \) deliver the positive pulse to the output when the SPWM logic status is high. On the other hand, the \( S \)PWM is active low to drive the switches 2 \( S \) and 4 \( S \) for negative pulse of the output signal. At the same time, the \( S \)PWM logic and the cycle logic dictate the switching operation for the desired input power factor. When the Cycle signal is high, the switches 1 \( S \) and 2 \( S \) are employed to control the input current for the positive cycle of the input voltage. For the negative cycle of the input voltage, the Cycle is active low to enable the switches 3 \( S \) and 4 \( S \) for input current control.

5. CIRCUIT BREAKER

5.1 Introduction

A circuit breaker is an automatically operated electrical switch designed to protect an electrical circuit from damage caused by over load or short circuit. Its basic function is to detect a fault condition and interrupt current flow. Unlike a fuse, which operates once and then must be replaced, a circuit breaker can be reset (either manually or automatically) to resume normal operation. Circuit breakers are made in varying sizes, from small devices that protect an individual household appliance up to large switchgear designed to protect high voltage circuits feeding an entire city.

5.2 Operation

All circuit breaker systems have common features in their operation, although details vary substantially depending on the voltage class, current rating and type of the circuit breaker. The circuit breaker must detect a fault condition; in low voltage circuit breakers this is usually done within the breaker enclosure. Circuit breakers for large currents or high voltages are usually arranged with protective relay pilot devices to sense a fault condition and to operate the trip opening mechanism. The trip solenoid that releases the latch is usually energized by a separate battery, although some high-voltage circuit breakers are self-contained with current transformers, protective relays and an internal control power source.

Once a fault is detected, contacts within the circuit breaker must open to
interrupt the circuit; some mechanically-stored energy (using something such as springs or compressed air) contained within the breaker is used to separate the contacts, although some of the energy required may be obtained from the fault current itself. Small circuit breakers may be manually operated, larger units have solenoids to trip the mechanism, and electric motors to restore energy to the springs. The circuit breaker contacts must carry the load current without excessive heating, and must also withstand the heat of the arc produced when interrupting (opening) the circuit. Contacts are made of copper or copper alloys, silver alloys and other highly conductive materials. Service life of the contacts is limited by the erosion of contact material due to arcing while interrupting the current. Miniature and molded-case circuit breakers are usually discarded when the contacts have worn, but power circuit breakers and high-voltage circuit breakers have replaceable contacts. When a current is interrupted, an arc is generated. This arc must be contained, cooled and extinguished in a controlled way, so that the gap between the contacts can again withstand the voltage in the circuit. Different circuit breakers use vacuum, air, insulating gas or oil as the medium the arc forms in. Different techniques are used to extinguish the arc including

- Lengthening / deflection of the arc
- Intensive cooling (in jet chambers)
- Division into partial arcs
- Zero point quenching (Contacts open at the zero current time crossing of the AC waveform, effectively breaking no load current at the time of opening. The zero crossing occurs at twice the line frequency, i.e. 100 times per second for 50 Hz and 120 times per second for 60 Hz AC)
- Connecting capacitors in parallel with contacts in DC circuits.

Finally, once the fault condition has been cleared, the contacts must again be closed to restore power to the interrupted circuit.

6. SIMULATION RESULTS

A computer simulation has been carried out to examine the performance of the proposed system. Simulation results confirm the validity of the control algorithms including, input current control, power factor correction, dc-link voltage control, and output current control. The parameters in the proposed system shown in Fig. 6.1 are summarized in Table III.

<table>
<thead>
<tr>
<th>Parameters</th>
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<tbody>
<tr>
<td>$L_1$</td>
<td>1.5mH</td>
<td>$V_1$</td>
<td>220Vrms/50Hz</td>
</tr>
<tr>
<td>$C_1$</td>
<td>6.000µF</td>
<td>$i_{in}$</td>
<td>0-600A/50, 60 Hz</td>
</tr>
<tr>
<td>$C_2$</td>
<td>6.000µF</td>
<td>$V_{C1}$</td>
<td>400V</td>
</tr>
<tr>
<td>$f_1$</td>
<td>20kHz</td>
<td>$V_{C2}$</td>
<td>400V</td>
</tr>
</tbody>
</table>

Fig. 6.2 shows the simulation results for steady-state response of the input current where the dc reference signal is set to 400 V. The input current, $s\ i$, is sinusoidal and in phase with the input voltage. Fig. 6.3 shows the simulated steady-state behavior of the system with the reference set at 200 A(rms). Fig. 6.4 shows the simulation results for a step response of the output current from 100 to 200 A(rms). Once the output current is increased, the dc-link capacitor voltage decreases. The PFC controller increases the input current to regulate the dc-link capacitor voltage at the targeted value. Fig. 6.5
shows simulation results for steady-state response of the output current control at 60 Hz, 100 A(rms) which is differed from the input line frequency at 50 Hz. Next, the simulation results of the current controls according to CB test case (a) where the test current is ramped from zero to 1.13In and the test case (d) where the test current is stepped from zero to 3In are demonstrated. A type-B CB with the current rating at 50 A is used as a device under test and the simulation results for test cases (a) and (d) are given in Figs. 6.6 and 6.7, respectively. Note that the tripping mechanism of the CB is not shown in the simulation study.

Fig 6.1 Simulation diagram

Fig 6.2. DC-link voltage (C1V and C2V) at 400 V and ac input voltage (sv) and current (si) waveforms.

Fig. 6.3. Output current control at 200 Arms.

Fig. 6.4. Response to step change of ac output current from 100 to 200 Arms.

Fig. 6.5. Output current at 100 A(rms) with the frequency of 60 Hz.

Fig. 6.6. Ramped current (0 to 56.5 Arms) for test case a).

Fig. 6.7. Test current at 150 Arms for test case d).

CONCLUSION

In this paper, the novel single-phase ac-ac converter with ac output...
current controls is proposed and digitally implemented according to the circuit-breaker (CB) testing standard (IEC 60898). Both simulation and experimental results show the improved transient step current control performance over the traditional ac current source based on the motor driven tap changing of auto-transformer. The proposed system is simple and low cost with minimum number of switches employed. The boost PFC topology with dual dc-link voltage controls is also incorporated in the proposed system. A laboratory prototype rated 600A(rms) output was constructed to verify the proposed system. According to results, the proposed topology accomplishes the sinusoidal input line current with unity power factor and low THDi of output current. The satisfactory transient step responses of output current are obtained.

REFERENCES


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JNTUH Hyderabad, He has a teaching experience of 12 years. He installed and supervised a Bloom Energy box of generating capacity 200W and also researched area includes Non conventional energy systems and Power systems. His areas of interest are Power Semiconductor devices and the application of power electronics in power systems.
Control Of DC Voltage In Multi-Terminal VSC HVDC Systems With Fuzzy Logic Controller

Harika and G.Anil
Jayamukhi Institute of Technological Sciences

Abstract
This particular cardstock looks at this extendable of electromechanical stability models of voltage supplier converter large voltage immediate present (VSC HVDC) to be able to multi-terminal (MTDC) devices. The cardstock presents a new management model having a cascaded DC voltage management at every converter that enables a new two-terminal VSC HVDC system to deal with converter failures. Any time expanded a great MTDC system, this model by natural means changes in to a master-slave set-up together with converters taking over this DC voltage management in the event this DC voltage curbing converter neglects. It is found how the model can often will include a voltage flagg management to share with you the energy difference from a concurrent within the DC system between the converters within the system. Eventually, this cardstock looks at a couple of achievable model savings, in line with the presumptions made in transient stableness modeling. The management algorithms and also VSC HVDC devices have been put in place using both equally MatDyn, a good start supplier MATLAB transient stableness system, along with the industrial electrical power system simulation bundle EUROSTAG.

1 Introduction
Over the last decade, the power engineering world is showing an increasing interest in voltage source converter high voltage direct current (VSC HVDC) technology. In Europe, suggestions have even been made to construct a new overlay DC grid based on VSC HVDC technology [1]. With these prospects of extending the principles of VSC HVDC to multi-terminal (MTDC) configurations, the modeling and control of MTDC systems has become one of the more prominent research topics. This paper introduces a generic electromechanical stability model for MTDC systems with a distributed DC voltage control. The focus of the paper is on the DC system itself and not on the interconnected AC/DC system.

When modeling the MTDC system, a distinction is traditionally made based on the level of modeling detail. Electro-Magnetic Transient Programs (EMTP) accurately represent the switching dynamics and electromagnetic transients. Averaged models and electromechanical stability models [2] have been used to study alternative outer controller structures ], and optimized control settings [as well as dynamic interaction with the AC system and system frequency support. Power flow algorithms, as presented in, have been used to address the steady-state effects of a distributed DC voltage control. Significant work has already been carried out on the modeling and control of MTDC systems. With the DC system voltage being the most crucial control variable, most focus has been dedicated towards a distributed control of
the DC voltage at different converters. The two main control methods are voltage margin control] and DC voltage droop control.

This paper builds upon the fundamental frequency modeling approach presented in [2]. Two important extensions are added to the model. Firstly, current and voltage limits are represented in detail in the current control loop and in the outer controller. Secondly, a cascaded control structure is introduced in the outer controller which allows power controlling converters to take over the voltage control when the DC voltage controlling converter fails. The main innovation is that this cascaded control structure for a two-terminal system, developed in the framework of this paper, is extended in a systematic way to obtain a generalized cascaded control scheme for MTDC systems. This generalized cascaded control scheme can accommodate for voltage margin control as well as for voltage droop control. The second contribution of the paper is the investigation of the effect of the detailed modeling of the current and voltage limits, by comparing the detailed model with a simplified model. The model has been developed and implemented in MatDyn [18] at KU Leuven and implemented and tested in EUROSTAG [19] at Tractebel Engineering.

2. HIGH-VOLTAGE, DIRECT CURRENT (HVDC)

A high-voltage, direct current electric power transmission system uses direct current for the bulk transmission of electrical power, in contrast with the more common alternating current (AC) systems. For long-distance transmission, HVDC systems may be less expensive and suffer lower electrical losses. For underwater power cables, HVDC avoids the heavy currents required to charge and discharge the cable capacitance each cycle. For shorter distances, the higher cost of DC conversion equipment compared to an AC system may still be warranted, due to other benefits of direct current links. HVDC allows power transmission between unsynchronized AC transmission systems. Since the power flow through an HVDC link can be controlled independently of the phase angle between source and load, it can stabilize a network against disturbances due to rapid changes in power. HVDC also allows transfer of power between grid systems running at different frequencies, such as 50 Hz and 60 Hz. This improves the stability and economy of each grid, by allowing exchange of power between incompatible networks.

High voltage is used for electric power transmission to reduce the energy lost in the resistance of the wires. For a given quantity of power transmitted, doubling the voltage will deliver the same power at only half the current. Since the power lost as heat in the wires is proportional to the square of the current for a given conductor size, but does not depend on the voltage, doubling the voltage reduces the line losses per unit of electrical power delivered by a factor of 4. While power lost in transmission can also be reduced by increasing the conductor size, larger conductors are heavier and more expensive.

The first long-distance transmission of electric power was demonstrated using direct current in 1882 at Miesbach-Munich Power Transmission, but only 1.5 kW was transmitted. An early method of high-voltage DC transmission...
was developed by the Swiss engineer René Thury and his method was put into practice by 1889 in Italy by the Acquedotto De Ferrari-Galliera company. This system used series-connected motor-generator sets to increase the voltage. Each set was insulated from electrical ground and driven by insulated shafts from a prime mover. The transmission line was operated in a 'constant current' mode, with up to 5,000 volts across each machine, some machines having double commutators to reduce the voltage on each commutator. This system transmitted 630 kW at 14 kV DC over a distance of 120 km. The Moutiers-Lyon system transmitted 8,600 kW of hydroelectric power a distance of 200 km, including 10 km of underground cable. This system used eight series-connected generators with dual commutators for a total voltage of 150,000 volts between the positive and negative poles, and operated from c.1906 until 1936. Fifteen Thury systems were in operation by 1913. Other Thury systems operating at up to 100 kV DC worked into the 1930s, but the rotating machinery required high maintenance and had high energy loss. Various other electromechanical devices were tested during the first half of the 20th century with little commercial success.

3. CONVERTER AND DC GRID MODELING

The converter can be modeled as a controllable voltage source behind a complex impedance connected to the point of common coupling (PCC), as shown in Fig. 1. This complex impedance comprises both the converter reactance and the transformer.

Transforming the three-phase equations to a rotating reference frame and assuming the grid voltage to be entirely oriented in the -direction, the converter equations become
The assumption that the voltage at the PCC is entirely aligned with the $q$-axis comes down to neglecting the effect of the phase locked loop (PLL). A first order system model the time delay caused by the processing and computation of the data and switching of the converter power electronics.

$$R_c i_{cq} + L_c \frac{di_{cq}}{dt} = u_{cq} - \omega L_c i_{cd} - u_{sq}$$

$$R_c i_{cd} + L_c \frac{di_{cd}}{dt} = u_{cd} + \omega L_c i_{cq}.$$  

A similar expression holds for $q$. Fig. 2 schematically depicts the model. The DC lines are represented by a lumped - equivalent scheme, as depicted in Fig. 3. The DC voltage dynamics at bus are determined by [2]

$$C_{dc,1} \frac{du_{dc,1}}{dt} = i_{dc,1} + \sum_{j=1}^{i-1} i_{dc,ij} - \sum_{j=i+1}^{N} i_{dc,ij}$$

with $C_{dc,i} = C_{dc,1} + \sum_{j=1}^{N} \frac{C_{dc,ij}}{2}$

with and respectively the DC voltage and current at bus the converter DC capacitance, the current in the branch between buses and and the branch capacitance. When the DC current dynamics are taken into account by modeling lumped inductances as shown in Fig. 3, the current dynamics of the branches connected to bus are modeled by

$$L_{dc,ij} \frac{di_{dc,ij}}{dt} + R_{dc,ij} i_{dc,ij} = u_{dc,1} - u_{dc,j}, \forall 1 \leq j \leq N$$

with and the DC branch resistance and inductance. When the DC current dynamics are neglected, as discussed in Section V, the currents are eliminated as state variables.

### 3.2 Two-Terminal VSC HVDC Control

This section recapitulates the control of a two-terminal scheme, a full detailed description can be found in [20]. The first part briefly summarizes the decoupled current control current controller. principles, with emphasis on the converter voltage limits. The second part discusses different outer control loops. The third part proposes an alternative implementation using a cascaded structure of an active power controller and DC voltage controllers at the two converters in order to increase overall redundancy.

![Converter model block diagram.](image1)

![DC side lumped parameter model.](image2)

![Decoupled inner current controllers.](image3)

**A. Decoupled Current Control**

The VSC is controlled in a rotating -reference frame that is synchronized with
the system voltage. Fig. 4 shows the inner current controllers, including an anti-windup (AWU). The voltage limits and are determined by the maximum modulation factor and the DC voltage. The maximum converter voltage magnitude can thus be written as

\[ u_{c_{\text{lim}}} = m_{\text{max}} u_{dc} \]

The limits can be implemented such that the controller can give priority to active or reactive power control. With the decoupling terms defined as

\[ \Delta u_{c_q} = \omega L_c i_{c_d} \]

\[ \Delta u_{c_d} = -\omega L_c i_{c_q} \]

a modified -decoupling term can be defined as

\[ \Delta u_{c_q}^+ = \Delta u_{c_q} + u_{c_r} \]

When under voltage limitation, the terms and are prioritized over the voltages that are used to control the currents. When prioritizing active over reactive power control, the -limit can be written as

\[ u_{c_{q_{\text{lim}}}} = \begin{cases} \sqrt{u_{c_{\text{lim}}}^2 - \Delta u_{c_d}^2} & \text{if } |\Delta u_{c_q}^+| \leq u_{c_{q_{\text{lim}}}} \\ \sqrt{1 + \left( \frac{\Delta u_{c_q}^+}{\Delta u_{c_d}} \right)^2} & \text{if } |\Delta u_{c_q}^+| > u_{c_{q_{\text{lim}}}} \end{cases} \]

with the modified decoupling vector defined as The voltage limit in the -axis, , can consequently be expressed as

\[ u_{c_{d_{\text{lim}}}} = \sqrt{u_{c_{\text{lim}}}^2 - u_{c_{q_{\text{lim}}}}^2} - u_{c_{r_{\text{lim}}}} \]

Alternatively, equal priority can be given to both - and components by having

\[ u_{c_{q_{\text{lim}}}} = \sqrt{\frac{u_{c_{\text{lim}}}^2}{1 + \left( \frac{u_{c_{q_{\text{lim}}}}}{u_{c_{r_{\text{lim}}}}} \right)^2}} \text{ if } |\Delta u_{c_q}^+| > u_{c_{q_{\text{lim}}}} \]

\[ u_{c_{d_{\text{lim}}}} = \sqrt{\frac{u_{c_{\text{lim}}}^2}{1 + \left( \frac{u_{c_{d_{\text{lim}}}}}{u_{c_{q_{\text{lim}}}}} \right)^2}} \text{ if } |\Delta u_{c_d}^+| > u_{c_{d_{\text{lim}}}} \]

when under voltage limitations. In these expressions, is the value of the converter voltage references before limiting, as shown in Fig. 4.

B. Standard Two-Terminal Outer Control

The current control components and are physically linked to the active and reactive power that the VSC injects in the AC system. Fig. 5 shows the outer active and reactive power PI-controllers. As an alternative to the reactive power controller shown in Fig. 5(b), one can use the -axis current to directly control the voltage at the AC terminal. Reactive power control is not the main focus of this paper and will not be discussed further. In a two-terminal scheme, one converter controls the active power (Fig. 5(a)) whereas the other controls the DC voltage at its DC bus (Fig. 6). When giving priority to active power over reactive power control, the current - and -limits, respectively, and in Figs. 5 and 6, are given by

\[ P_{\text{lim}} = K_p \left( 1 + \frac{1}{\tau_{c_p}} \right) \]

\[ Q_{\text{lim}} = K_q \left( 1 + \frac{1}{\tau_{c_q}} \right) \]

Fig. 5. Outer active and reactive power controllers. (a) Constant controller. (b) Constant controller.

\[ u_{c_{\text{lim}}} = K_{c_{\text{dc}}} \left( 1 + \frac{1}{\tau_{c_{dc}}} \right) i_{c_{q_{\text{lim}}}} \]

\[ i_{c_{\text{lim}}} \leq i_{c_{q_{\text{lim}}}} \]

Fig. 6. Outer DC voltage controller.
Alternatively, equal priority can be given to the active and reactive power control, by having

\[ i_{cclim} = \frac{i_{cclim}}{\sqrt{1 + \left(\frac{i_{cclim}}{i_{cclim}}\right)^2}} \text{ if } |i_{cclim}| > i_{cclim} \]

\[ i_{cclim} = \frac{i_{cclim}}{\sqrt{1 + \left(\frac{i_{cclim}}{i_{cclim}}\right)^2}} \text{ if } |i_{cclim}| > i_{cclim} \]

with the current reference before limiting, as shown in Figs. 5 and 6. Instead of giving equal priority to both control components, this formulation can be generalized to prioritize one current component over the other, without completely compromising the other, by defining a constant ratio such that

\[ i_{cclim} = \frac{i_{cclim}}{\sqrt{1 + \alpha^2}} \text{ if } |i_{cclim}| > i_{cclim} \]

\[ i_{cclim} = \frac{i_{cclim}}{\sqrt{1 + \left(\frac{i_{cclim}}{i_{cclim}}\right)^2}} \text{ if } |i_{cclim}| > i_{cclim} \]

When observing the steady-state behavior of a converter when under current limits, (15)–(16) results in the absence of any reactive power injected by the converter. The approach from (19)–(20) results in an operation at constant power factor such that

\[ \cos \phi_c = \frac{1}{\sqrt{1 + \alpha^2}}. \]

This implementation guarantees operation at constant power factor and can be of interest when the reactive power support provided to the AC network has to be guaranteed when a converter limit is hit. The implementation from (15)–(16) prioritizes active power, which makes it a suitable candidate for use in a DC voltage controlling converter. The steady-state behavior resulting from (17)–(18) on the contrary, depends on the values of the current reference before limiting. The reference currents are also reduced under AC fault conditions, to limit the short circuit contribution by the converter [21].

Fig.3. 7. Combined active power and DC voltage controller.

This can be easily included by having when the voltage at the PCC drops. Instead of limiting the currents under fault conditions, the priority can also be shifted to reactive power control to fulfill the grid code requirements concerning voltage support [22].

C. Redundant Outer Control

One of the disadvantages of the control implementation from the previous part, is that the control structure as such cannot cope with an outage or blocking of the DC voltage controlling converter. Whereas an outage or blocking of the power controlling converter only causes the power to drop, it does not cause a system outage since the DC voltage controlling converter can still control the DC voltage. As the control of the DC voltage is crucial to the operation of the power system, one can therefore duplicate the DC voltage control, as proposed in [21] and elaborated in [23] for the power synchronization control, and mentioned in [24] for the operation of a two-terminal scheme. Fig. 7 shows the control structure for such a cascaded power control that has been developed in the framework of this paper. By implementing a correct control structure depending on the DC voltage at
the converter's DC terminal, it is guaranteed that only one converter at a time controls the DC voltage.

In the power controlling converter, the DC voltage is used both as a reference signal and feedback signal as shown in Fig. 7, hence only is retained as an input to the DC voltage controller. By using the actual DC voltage instead of a reference value, one avoids counteracting actions of the DC voltage controller when the DC voltage varies as a result of an active power or DC voltage set-point change at another converter in the system.

The controller ensures that the power is controlled as long as the voltage stays within the limits and . As soon as the voltage drops below or raises above , the controller switches to voltage control, controlling the voltage to one of the reference values, respectively and . This is expressed mathematically as

\[ u_{d0} = \begin{cases} u_{d0 \text{min}} & \text{if } u_{d0} \leq u_{d0 \text{min}} \\ u_{d0} & \text{if } u_{d0 \text{min}} < u_{d0} < u_{d0 \text{max}} \\ u_{d0 \text{max}} & \text{if } u_{d0} \geq u_{d0 \text{max}} \end{cases} \]

with and and a voltage deadband. As soon as the DC voltage reference changes to either or is set to zero and the AWU of the active power PI-controller is activated to avoid an overshoot when the control switches back to active power mode. The deadband prevents oscillating between the two different operational regimes. The DC voltage can start increasing or decreasing as a result of a power outage of the DC voltage controlling converter. By providing a cascaded structure with an inner DC voltage control as described above, a backup control is provided in case the DC voltage controlling converter fails. The remaining converter can now continue to operate as a STATCOM. In the next section, this cascaded general control structure will be used in an MTDC network.

![Fig. 3.8. Initial conditions of the test system.](image)

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![Fig. 3.9. Interactions of converters in the DC grid after outage of converter 2: (a) Active power to the AC grid and (b) DC voltage (MatDyn simulation, including ).](image)

IV. MULTI-TERMINAL VSC HVDC CONTROL

A. Voltage Margin Control

When the redundant control structure from the previous section is used in a multi-terminal configuration, it operates as a so called voltage margin control [5] scheme, providing a backup DC slack converter in case the main slack converter (or DC voltage controlling converter) fails. Fig. 10 shows the steady state P-V characteristics resulting from the control implementation as observed from the DC side, thereby neglecting the converter losses. is the active power limit resulting from the limit discussed in Section III. Consequently, the actual
value of depends on the voltage at the AC bus and the ratio. The voltage margin at different converters can be determined such that different converters can take over the DC voltage control, given that only one converter at a time can control the DC voltage.

Contrary to the two-terminal system, it is still possible to transfer power in case the DC slack converter fails or blocks. Fig. 9 shows simulation results for the voltage margin control implemented in the 4-terminal VSC HVDC system from Fig. 8 using MatDyn, an open-source MATLAB-based transient stability program [18]. A modified Euler ODE solver was used with a step size of 2e-4 s. The initial power flow solution from Fig. 8, with the DC slack converter at bus 2, has been obtained using MATACDC, an open-source MATLAB-based AC/DC power flow program [25]. The power flow has been initialized such that the average voltage is equal to unity. After the outage of the DC voltage controlling converter 2, converter 3 initially tries to control the converter voltage when its converter upper voltage limit is reached. Since its current limit is hit, converter 3 is unable to control the converter voltage further, resulting in a further increase of the DC system voltage, after which converter 1 takes over the voltage control. The power in converter 4 remains unchanged because the influence of the changing DC voltage is not fed back to the power controlling converters as long as the voltage limits are not hit (Fig. 7).

B. Voltage Droop Control

Alternatively, the voltage control can be distributed amongst different converters by implementing a voltage droop control[17]. Fig. 11 shows how the droop control can be integrated in the redundant control structure from Fig. 7 (shown in gray). Contrary to standard droop control schemes presented in literature, which do not contain an inner DC voltage control loop, cascading the droop control as done in this paper has the advantage that upper and lower DC voltage limits can still be included as for 2-terminal schemes, ensuring that the DC voltage can still be controlled in case a converter is operating in islanding mode, e.g., as a result of DC breaker actions. The DC droop control can be implemented by letting

\[ P_s^* = P_s^0 + \frac{1}{K_{dc}}(u_{dc} - u_{dc,0}) \]

with \( P_s^0 \), the reference active power, depending on the set points of active power and DC voltage and the droop factor.
In [6], an alternative approach has been proposed to use an adaptive droop control based on a common voltage feedback signal instead of a local voltage measurement, thereby requiring communication. The droop values can be optimized taking into account the DC system dynamics, as done in [8] or both the AC and DC system dynamics, as in [6].

Fig. 4.5 shows the steady-state characteristics of the DC voltage droop when implemented as shown in Fig. 11. Similarly to the voltage margin control, results from the \( P \)-limit. The \( u \)-limits can be included at some converter stations to prevent the voltage from decreasing or increasing at a certain point. By setting and respectively low and high enough, such that the \( u \)-limit is hit before hitting or , no voltage limits are active. Figs. 12 and 13 show the results for the voltage droop control after an outage of converter 2, assuming a 1 p.u. power change corresponding to a 10% voltage drop/increase. The results were respectively obtained using MatDyn and EUROSTAG. EUROSTAG uses an advanced symmetrically A-stable algorithm with variable step size that guarantees constant accuracy as well as high speed simulation [26]. In these simulations, the control scheme continues operating as a voltage droop scheme, since no voltage limits were hit at any of the converters. Similarly to the results in case of the voltage margin control in Fig. 9, converter 1 hits a current limit, which is accounted for by the other converter's droop action. The advantage of this voltage droop over the voltage margin control, is that the power after the converter outage is shared amongst the different droop controlled converters in the DC system, which makes the voltage droop control a suitable candidate for an operation in large DC grids. The joint control action of the different converters in the system also results in smaller voltage deviations.
5. Simulation result

CONCLUSION

In this paper, an over-all electromechanical multi-terminal VSC HVDC product may be shown. The salient highlights of the product tend to be that it incorporates a generalized cascaded command plan pertaining to MTDC programs that allows pertaining to voltage perimeter as well as voltage sag command understanding that recent as well as voltage restricts tend to be showed at length. A method to handle a new decrease of the voltage controlling converter inside a two-terminal process is usually generalized in order to voltage perimeter command pertaining to multi-terminal process and the product may be extensive to add in sent out DC voltage command. It is found by means of simulations what sort of restricts effect the design as well as what the results tend to be involving disregarding converter restricts. The final results indicate that will diminished buy designs close the detailed product effectively. The product may be implemented inside open-source, MATLAB-based layer, MatDyn, as well as inside a business electric power process simulation software, EUROSTAG, possesses recently been tested on a four-terminal VSC HVDC process.

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IMPROVE EFFICIENCY ON GRID FEEDING CURRENT SOURCE INVERTER FOR SOLAR PHOTOVOLTAIC SYSTEM

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Abstract
High efficiency and operating life of grid feeding solar photovoltaic (PV) inverters are demanded. Due to reduced dc-link capacitor requirement, current source inverter (CSI) offers higher reliability than the voltage source based solar inverter. However, conventional three-phase pulse width modulated (PWM) current source based solar inverter injects high earth leakage current into the grid. In order to suppress this current, an isolation transformer can be used. Use of this transformer increases the cost and size, and decreases overall efficiency. In order to address the aforementioned limitations, a modified CSI is proposed in this paper. The proposed inverter suppresses the earth leakage current without using an isolation transformer, thereby increasing the efficiency and reducing cost as compared to conventional current source based solar inverters. A mathematical model of the system is derived based on which controller for the operation of the inverter is designed. The effectiveness of the scheme is verified through detailed simulation study. To confirm the viability of the scheme, experimental studies are carried out on a scaled-down laboratory prototype.

1 Introduction
Depleting fossil fuels, increasing energy demand, and concern over climate change due to CO₂ emissions motivate the use of solar photovoltaic (PV). In grid feeding solar PV system, electricity generated by solar PV is fed to the grid without storage. Following are the major components of grid feeding solar PV system: (1) solar PV panels; (2) inverters; and (3) other balance of system (such as cables, mechanical structure support, shelters, etc). Life of solar PV panels is around 20 years. However, inverters are less reliable and typically have 3–7 years of life span, beyond which high failure rate of inverters is reported [1]. Failures of power electronic converters are mainly due to the following components: aluminum electrolytic capacitors (AEC); (2) switching semiconductor devices; and (3) inductive elements. As reported in, the primary factor, which limits the life of converters, is AEC. It is responsible for about 60–70% of the total failures.

This value is expected to be higher for “string” (low/medium power) solar PV inverters, due to exposure to high ambient temperature. Considering the aforementioned reasons, alternatives to conventional AEC are investigated. Derated AECs are capable of operating at high temperatures, thereby improving reliability of the system. Solid film type ac capacitors also offer high reliability as compared to conventional AEC. However, size and cost of these alternatives are higher than those of AEC. Existing solar (string) inverters are based on voltage source inverter (VSI) topology. Considering the high current ripple supplied/absorbed by the dc-link capacitor in VSI, large value of capacitance is required to limit the voltage ripple across
solar PV terminals. Therefore, alternatives suggested above may not be economically viable. Alternatively, in current source inverter (CSI) topology, dc-link inductor limits the ripple in dc current to a low value. Therefore, current supplied/absorbed by the capacitor has less ripple due to additional current smoothing action of the dc-link inductor. Therefore, CSI requires smaller dc-link capacitor, thereby facilitating the use of highly reliable capacitor. Therefore, current source based solar inverters will have longer operational life as compared to voltage source based solar inverters. In addition to high reliability, solar inverter should also have high efficiency of power conversion.

However, in case of CSI, both dc-link inductor and dc-link capacitor collectively determine the ripple in dc voltage. Therefore, low value of voltage ripple can be achieved by suitable selection of dc inductor. Thus, low capacitance values in CSI do not affect the MPPT. Use of three-phase pulse width modulated (PWM) CSI for solar PV application is suggested in. The use of space vector modulation technique for grid feeding CSI is discussed in, while in, issues related to control and MPPT are discussed. Modeling of CSI for PV application is reported in, and the use of one cycle controller for this inverter is suggested in. However, these inverters generate high common mode voltage, which forces common mode earth leakage current.

2.GRID-TIE INVERTER

2.1 Introduction

A grid-tie inverter is a power inverter that converts direct current (DC) electricity into alternating current (AC) with an ability to synchronize to interface with a utility line. Its applications are converting DC sources such as solar panels or small wind turbines into AC for tying with the grid.

Residences and businesses that have a grid-tied electrical system are permitted in many countries to sell their energy to the utility grid. Electricity delivered to the grid can be compensated in several ways. "Net metering" is where the entity that owns the renewable energy power source receives compensation from the utility for its net outflow of power. So for example, if during a given month a power system feeds 500 kilowatt-hours into the grid and uses 100 kilowatt-hours from the grid, it would receive compensation for 400 kilowatt-hours. In the US, net metering policies vary by jurisdiction. Another policy is a feed-in tariff, where the producer is paid for every kilowatt hour delivered to the grid by a special tariff based on a contract with distribution company or other power authority. In the United States, grid-interactive power systems are covered by specific provisions in the National Electric Code, which also mandates certain requirements for grid-interactive inverters.

2.2 Typical operation

Inverters take DC power and invert it to AC power so it can be fed into the electric utility company grid. The grid tie inverter must synchronize its frequency with that of the grid (e.g. 50 or 60 Hz) using a local oscillator and limit the voltage to no higher than the grid voltage. A high-quality modern GTI has a fixed unity power factor, which means its output voltage and current are perfectly lined up, and its phase angle is within 1 degree of the AC power grid. The inverter has an on-board computer which will sense the
current AC grid waveform, and output a voltage to correspond with the grid. However, supplying reactive power to the grid might be necessary to keep the voltage in the local grid inside allowed limitations. Otherwise, in a grid segment with considerable power from renewable sources voltage levels might rise too much at times of high production, i.e. around noon.

Grid-tie inverters are also designed to quickly disconnect from the grid if the utility grid goes down. This is an NEC requirement that ensures that in the event of a blackout, the grid tie inverter will shut down to prevent the energy it transfers from harming any line workers who are sent to fix the power grid. Properly configured, a grid tie inverter enables a homeowner to use an alternative power generation system like solar or wind power without extensive rewiring and without batteries. If the alternative power being produced is insufficient, the deficit will be sourced from the electricity grid.

Fig 2.1 Inverter for grid-connected PV

3.PHOTOVOLTAIC POWER SYSTEM

3.1 Introduction

Photovoltaics (PV) is the name of a method of converting solar energy into direct current electricity using semiconducting materials that exhibit the photovoltaic effect, a phenomenon commonly studied in physics, photochemistry and electrochemistry. A photovoltaic system employs solar panels composed of a number of solar cells to supply usable solar power. The process is both physical and chemical in nature, as the first step involves the photoelectric effect from which a second electrochemical process take place involving crystallized atoms being ionized in a series, generating an electric current. Power generation from solar PV has long been seen as a clean sustainable energy technology which draws upon the planet’s most plentiful and widely distributed renewable energy source – the sun. The direct conversion of sunlight to electricity occurs without any moving parts or environmental emissions during operation. It is well proven, as photovoltaic systems have now been used for fifty years in specialized applications, and grid-connected PV systems have been in use for over twenty years. They were first mass-produced in the year 2000, when German environmentalists including Eurosolar succeeded in obtaining government support for the 100,000 roofs program.

Driven by advances in technology and increases in manufacturing scale and sophistication, the cost of photovoltaics has declined steadily since the first solar cells were manufactured, and the levelised
cost of electricity from PV is competitive with conventional electricity sources in an expanding list of geographic regions. Net metering and financial incentives, such as preferential feed-in tariffs for solar-generated electricity, have supported solar PV installations in many countries. With current technology, photovoltaics recoups the energy needed to manufacture them in 1.5 to 2.5 years in Southern and Northern Europe, respectively.

Fig 3.1 The Solar Settlement, a sustainable housing community project in Freiburg, Germany.

Fig 3.2 Photovoltaic SUDI shade is an autonomous and mobile station in France that provides energy for electric vehicles using solar energy.

Fig 3.3 Solar panels on the International Space Station

For best performance, terrestrial PV systems aim to maximize the time they face the sun. Solar trackers achieve this by moving PV panels to follow the sun. The increase can be by as much as 20% in winter and by as much as 50% in summer. Static mounted systems can be optimized by analysis of the sun path. Panels are often set to latitude tilt, an angle equal to the latitude, but performance can be improved by adjusting the angle for summer or winter. Generally, as with other semiconductor devices, temperatures above room temperature reduce the performance of photovoltaics.

4. COMMON MODE EARTH LEAKAGE CURRENT

4.1 Introduction

Metallic frames are used to provide mechanical strength and support to the PV modules. Due to large overlap surface area between PV cell and frame, parasitic capacitance is present between them. Further, the metallic frames are connected to earth (grounded) for safety. Therefore, parasitic capacitors (Cp1 and Cp2) are present between terminals of PV module and earth, as shown in Fig. 4.1. Value of these capacitors varies with ambient temperature, humidity, dust, and other environmental conditions. In case of crystalline and multi crystalline panels, this value may range from 50 nF/kWp to 150 nF/kWp, while for thin film solar PV cells, this value is around 1 μF/kWp. Terminals of PV panel are connected to the input of inverter. The inverter can be either directly connected to ac grid or through an isolation transformer as shown in Fig. 4.1(a) and (b), respectively. In the latter case either negative or positive using isolation transformer. terminal of input dc can be connected to earth. Therefore, voltages appearing across the parasitic capacitors, Cp1 and Cp2 are dc. For instance, if negative terminal of PV is connected to earth as shown in Fig. 1(b), voltage across Cp1 is 0 V and that across Cp2 is equal to Vdc. Therefore, no current
flows through the parasitic capacitance to earth. In case of a transformer-less system as shown in Fig.4.1(a), neither negative nor positive terminal of PV can be directly connected to earth. This is because, grid neutral is connected to earth at the substation, and potential difference between terminals of PV (either -ve or +ve terminal) and neutral depends on the conducting state of the inverter switches. Therefore, connecting PV terminals to earth will inject high earth fault currents. On the other hand, if PV terminals are not earthed, high (switching) frequency voltage appears across Cp1 and Cp2. This results in the flow of high earth leakage current. To demonstrate the generation of high-frequency common mode voltage and corresponding current, a conventional PWM-CSI based solar PV system, shown in Fig. 4.2, is simulated using MATLAB/Simulink platform. Parameters used for the simulation study are given in Table I. Space vector PWM technique reported in is used to generate gating signals, and simulated results are shown in Fig. 4.3.

Though dc-link voltage is maintained at 300 V, voltage across the PV terminals and earth has both dc and high-frequency ac components. This high-frequency ac is due to the switching action of the inverter devices. Harmonic spectrum of parasitic capacitor voltage vp2 is shown in Fig.4.4. The magnitude of the dominant harmonic voltage and the corresponding earth leakage current, considering parasitic capacitance of PV module as 50 nF/kWp, is given in Table II. Standard DIN VDE 0126-1-1 defines the limits on the common mode earth leakage currents to be 300 mA for grid-connected solar PV systems [17]. Immediate disconnection of inverter is recommended if leakage current exceeds this limit. It can be seen that the values for high frequency components given in Table II are higher than that specified by DIN VDE 0126-1-1. Therefore, conventional transformer-less, three-phase, PWM-CSI is not suitable for feeding power to the grid. To address this limitation, a modified CSI is proposed in this paper.

4.2 Modified Three-Phase CSI

The proposed CSI is shown in Fig.4.5. String of PV modules is connected across the input dc capacitors. The dc-link is realized by two capacitors, connected in series. Midpoint of these capacitors is connected to the neutral of the grid. DC-link inductors Ldc1 and Ldc2 are wound on the same core and therefore have a high

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**TABLE I PARAMETERS OF THE SIMULATED SYSTEM**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Value (in p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line voltage</td>
<td>400V</td>
<td>0.96</td>
</tr>
<tr>
<td>Grid frequency</td>
<td>50Hz</td>
<td>1</td>
</tr>
<tr>
<td>Inverter rating</td>
<td>10kW</td>
<td>1</td>
</tr>
<tr>
<td>AC filter inductor</td>
<td>400μH</td>
<td>7.3m</td>
</tr>
<tr>
<td>AC filter capacitor</td>
<td>100μF</td>
<td>0.54</td>
</tr>
<tr>
<td>DC-link inductor</td>
<td>2mH</td>
<td>7.3m</td>
</tr>
<tr>
<td>DC-link capacitor</td>
<td>25μF</td>
<td>7.3m</td>
</tr>
<tr>
<td>DC-link voltage</td>
<td>300V</td>
<td>1</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>7.5kHz</td>
<td></td>
</tr>
</tbody>
</table>

*J_{F \text{leak}}=10kW, V_{\text{dc}}=300V, V_{\text{AC}}=415V & f_{\text{samp}}=50Hz*
value of mutual coupling. To generate ac current waveforms from the dc current, eight semiconductor switching devices are used. Each device has unidirectional current flow capability and can block the reverse voltage. Either a diode connected in series with IGBT or reverse blocking (RB) IGBTs can be used to realize these switches. Output of three phases is connected to the grid through capacitor-inductor (C-L) filter and that of the fourth leg is connected to the neutral of the system as shown in Fig. 4.5. Components of the proposed inverter and their role in suppressing the earth leakage current are discussed below:

**TABLE II DOMINANT HARMONIC VOLTAGE AND CURRENT THROUGH PARASITIC CAPACITOR**

<table>
<thead>
<tr>
<th>Harmonic No.</th>
<th>Frequency</th>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>150Hz</td>
<td>155(V_{rms})</td>
<td>0.15A</td>
</tr>
<tr>
<td>147</td>
<td>7350Hz</td>
<td>75(V_{rms})</td>
<td>3.47A</td>
</tr>
<tr>
<td>150</td>
<td>7500Hz</td>
<td>116(V_{rms})</td>
<td>5.47A</td>
</tr>
<tr>
<td>153</td>
<td>7650Hz</td>
<td>68(V_{rms})</td>
<td>3.27A</td>
</tr>
</tbody>
</table>

**4.2.1 Common Mode Inductor**

Earth leakage current is of common mode nature and flows through both the +ve and -ve terminals of dc-link to the earth. Therefore, to reduce this current, common mode inductor is connected in the +ve and -ve dc-link. This inductor offers high impedance to the leakage current and reduces its magnitude. However, this addition does not eliminate the common mode voltage completely.

**4.2.2 Split Capacitor DC-Link**

Split capacitor dc-link is realized by connecting two capacitors in series. Midpoint of the link is connected to the system neutral. During operation, dc-link voltages \(v_{dc1}\) and \(v_{dc2}\) are maintained almost constant. Therefore, voltage difference between PV terminals and neutral wire is a constant dc value without high-frequency ac. Since neutral point is earthed at the substation, voltages across Cp1 and Cp2 are almost dc without high-frequency ac. Therefore, no high-frequency earth leakage current would flow. This technique is being used in VSI systems, where split capacitor arrangement is used to reduce the leakage current. However, in CSI, this arrangement results in undesirable inverter currents during the “zero state.” The reason for this behavior is explained in the following section.

**4.2.3 Fourth Leg**

Fig. 4.6 shows the reference waveform for inverter ac currents. The complete cycle is divided into six sectors. In sector-I, current reference for phase-A and phase-C is positive and that for phase-B is negative. To realize these reference currents, switches SA+, SA-, SB+, SB-, SC+, and SC− are modulated. Fig. 4.7(a) shows the current waveforms during a sampling period in sector-I. Solid lines are the average phase currents, and dotted lines indicate the instantaneous currents. The duration for which the switches are conducting in this sampling period is given by

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Fig. 4.6. Inverter reference current waveforms.

---

Fig. 4.5. Proposed current source based transformer-less solar inverter.
where, \( T_0 \) is the duration of zero state, and \( T_S \) is the sampling period. During zero state, both top and bottom switches of a leg are closed (in this case phase-B). Fig. 8(a) shows the equivalent circuit during this mode for a conventional CSI. No current should flow from inverter to the C–L filters, and dc inductor current increases due to PV voltage.

Fig. 4.7. Instantaneous and average current within a sampling period for (a) conventional CSI and (b) CSI with split capacitor.

Above equation gives the current flowing through phase-B and neutral during the zero state. Fig. 4.7(b) shows the flow of this additional current when phase-B voltage is negative. Due to current flow in phase-B during the zero state, average value of current during the sampling period deviates from the desired value as shown in Fig. 4.7(b). This current flow during the zero state is undesirable and should be restricted. In order to eliminate the flow of this current, additional pair of switches \( S_{N+} \) and \( S_{N-} \) are connected across the dc-link. Midpoint of this new leg is connected to the neutral. For the zero state, instead of closing both switches of a particular phase, these switches are closed. Therefore, no current flows from any phase to neutral during this duration.

5. PWM Technique

PWM technique for the proposed CSI should ensure the following conditions.
1) Maintain the continuity of dc current: At any instant, one of the four top switches SA+, SB+, SC+, or SN+ and one of the four bottom switches SA−, SB−, SC−, or SN− must be “ON.”

2) While turning “OFF” any switch, pulse delay or while turning “ON”, pulse advancement should be provided. This ensures that incoming switch is turned on before the outgoing switch turns off. Hence, current continuity is maintained. The delay and advancement are of very small duration as compared to the sampling period.

3) To force idc1 into the phase, top switch of that phase leg should be turned “ON.” Similarly, to force −idc2, bottom switch of that phase leg should be turned “ON.”

4) For zero current period, switches SN+ and SN− should be turned “ON.”

All the conditions except “4” are common for conventional PWM-CSI as well. Therefore, space vector PWM technique for three-phase CSI reported in [20] is suitably modified for the proposed topology.

6. SIMULATION STUDIES
In order to verify the efficacy of the proposed scheme, a 1.8 kW current source based grid feeding inverter is simulated on MATLAB/Simulink platform utilizing the parameters given in Table III. AC side filter is designed using the guidelines given in.

Simulated phase-a grid voltage vg−a, phase-a grid current ig−a, and phase-a inverter current ii−a are shown in Fig. 6.2. Inverter current leads the grid voltage, while grid current is in phase with grid voltage. Power factor of the injected power is 0.99, and THD of the current waveform is 4.22%. RMS value of the current injected in to the grid is 2.583 A, and dc current injected into the grid is about 10 mA, which is less than the limit specified in standards IEEE 929-2000 and IEEE 1547-2003. This confirms good steady-state performance of the proposed scheme. The simulated waveforms of vdc1, vdc2, idc1, and idc2 are shown in Fig. 6.3. The dc-link voltages are almost equal. Low-frequency oscillation is observed in dc capacitor voltages.

However, this ripple is out of phase in vdc1 and vdc2. Hence, it does not appear in the total dc-link voltage seen by the PV array, and it will not affect the performance of MPPT controller. Total dc-
link voltage is regulated at 300 V with less than 1% ripple. Both dc-link currents are found to be equal at 6 A. In order to evaluate the performance of the scheme, step change in reference value of dc voltage is initiated at 0.2 s. The performance of the scheme for the aforementioned case is shown in Fig.6.4. Stable operation of the system for large step change in the dc voltage demonstrates the robustness of the controller. Current drawn from PV array increases with decrease in voltage (due to I–V characteristics of PV array), thereby increasing the average dc-link current. Regulation of dc-link voltages at their corresponding reference values shows that the proposed dc-voltage controller is effective both during steady-state and transient conditions.

6.1 Efficiency Comparison
Efficiency of the proposed four-leg CSI is compared with that of conventional CSI in this section. Both conduction and switching losses are considered to evaluate efficiency. Full wave symmetrical modulation technique, discussed in, is considered for analyzing switching and conduction losses in both the topologies. Conduction losses: As discussed in Section III-D, at any instant, one of the four top switches carry idc1, and one of the four bottom switches carry idc2. Similarly, in conventional CSI, one of the three top switches carry idc, and one of the three bottom switches carry idc at any time. Since dc link current is same in both topologies (for same power delivered), total conduction losses remain same.

6.2 Switching losses
Since dc link current is same in both topologies, switching losses in CSI depend on the voltage appearing across the switch during turn-on and turn-off. Fig. 6.4(a) and (b) shows the switching states in conventional and four-leg CSI, respectively. Switching transitions in sector 1 for both the schemes are
Conventional CSI : (a+ a−) → (a+ b−) → (a+ c−) → (a+ a−)
Proposed 4 – leg CSI : (n+ n−) → (a+ b−) → (a+ c−) → (n+ n−).
split capacitor arrangement across the PV array, undesired current flows through the C-L filter during the zero state. To address this issue, two reverse blocking semiconductor switches are used as the fourth leg of CSI. Following are the techniques used to eliminate the flow of leakage current in the system.

1) Introduction of common mode inductor in the dc link offers high impedance to the flow of common mode leakage current.

2) Split capacitor arrangement and connection of neutral to midpoint of split capacitors eliminates high-frequency component from the common mode voltage, which in turn restricts the flow of common mode leakage current.

3) Addition of fourth leg avoids the possibility of undesired current flow through neutral or any phase during the zero state.

Key advantages of the proposed current source based transformer-less solar inverter are small dc capacitor, single stage conversion, and low leakage currents. A mathematical model of the system is developed to facilitate the design of controller. Detailed simulation studies are carried out to predict the performance of the system. In order to confirm the viability of the scheme, experimental studies are carried out utilizing a scaled-down laboratory prototype developed for the purpose.

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Improvement of Transient Response of DSTATCOM Using Fast Acting DC Link Voltage Controller

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Balaji Institute of Engineering and Sciences
Laknepally Narsampet

Abstract: The proliferation of power-electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power-quality (PQ) problems in the power distribution network. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion, high levels of neutral-to-ground voltage, and interference with communication systems. The shunt-connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it.

In this paper, a fast-acting dc-link voltage controller based on the energy of a dc-link capacitor is proposed. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The conventional PI controller used for maintaining the dc-link voltage. To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the difference between the actual and reference voltages. To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. Mathematical equations are given to compute the gains of the conventional controller based on fast-acting dc-link voltage controllers to achieve similar fast transient response. The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. The detailed simulation and experimental studies are carried out to validate the proposed controller. The efficiency of the proposed controller over the conventional dc-link voltage controller is established through the digital simulation.

1 Introduction

The proliferation of power-electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power-quality (PQ) problems in the power distribution network. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion, high levels of neutral-to-ground voltage, and interference with communication systems. The literature records the evolution of different custom power devices to mitigate the above power-quality problems by injecting voltages/currents or both into the system. The shunt-connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it.

One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature to compute the reference compensator currents. However, due to the simplicity in formulation and no confusion regarding the definition of powers, the control algorithm based on instantaneous symmetrical component theory is preferred. Based on this
algorithm, the compensator reference currents \( (i_{f_a}, i_{f_b}, i_{f_c}) \) are given as follows:

\[
\begin{align*}
    i_{f_a} &= i_{a} - \frac{\gamma}{\sqrt{3}} \frac{P_{av}}{v_z} \\
    i_{f_b} &= i_{b} - \frac{1}{\sqrt{3}} \frac{P_{av}}{v_z} \\
    i_{f_c} &= i_{c}
\end{align*}
\]

Where \( \gamma = \tan \phi / \sqrt{3} \phi \) is the desired phase angle between the supply voltages and compensated source currents in the respective phases. For unity power factor operation, \( \phi = 0 \), thus \( \gamma = 0 \). The term \( P_{av} \) is the dc or average value of the load power. The term \( P_{dc} \) in (1) accounts for the losses in the VSI without any dc loads in its dc link. To generate \( P_{dc} \), a suitable closed-loop dc-link voltage controller should be used, which will regulate the dc voltage to the reference value.

For the DSTATCOM compensating unbalanced and nonlinear loads, the transient performance of the compensator is decided by the computation time of average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of the average load power. Therefore, the transient performance of the compensator mostly depends on the computation of \( P_{av} \). In this paper, \( P_{av} \) is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics presence in voltages and currents. Although the computation of \( P_{dc} \) is generally slow and updated once or twice in a cycle, being a small value compared to \( P_{av} \), it does not play a significant role in transient performance of the compensator.

2. DISTRIBUTION STATIC COMPENSATOR (DSTATCOM)

2.1 Introduction

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the D-STATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor; and
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter.

Fig 2.1 - the shunt injected current \( I_{sh} \) corrects the voltage sag by adjusting the voltage drop across the system impedance \( Z_{th} \).

2.2 Mathematical Modeling Of Dstatcom

DSTATCOM is a shunt device which has the capability to inject or absorb both active and reactive current. The reactive power output of a D-STATCOM is proportional to the system voltage rather than the square of the system voltage, as in a capacitor. This makes DSTATCOM more suitable rather than using capacitors. Though storing energy is a problem for long term basis, considering real power compensation for voltage control is not an ideal case. So most of the operations considered is steady stat only and the power exchange in such a condition is reactive. To realize such a model,
It can be said that a DSTATCOM consists of a small DC capacitor and a voltage source converter.

![Fig 2.2 modeling of the dstatcom/ess:]

A DSTATCOM consists of a three-phase voltage source inverter shunt-connected to the distribution network by means of a coupling transformer, as depicted in Fig. 2.1. Its topology allows the device to generate a set of three almost sinusoidal voltages at the fundamental frequency, with controllable amplitude and phase angle. In general, the DSTATCOM can be utilized for providing voltage regulation, power factor correction, harmonics compensation and load leveling. The addition of energy storage through an appropriate interface to the power custom device leads to a more flexible integrated controller. The ability of the DSTATCOM/ESS of supplying effectively extra active power allows expanding its compensating actions, reducing transmission losses and enhancing the operation of the electric grid.

![Fig 2.3 Block diagram of the proposed DSTATCOM controller.]

Fig 2.3 shows the block diagram of the proposed DSTATCOM controller for the DSTATCOM. According to (11), the DSTATCOM controller calculates the compensation current commands by using line-to-line voltages and line current. The instantaneous compensation currents are obtained with the aid of the synchronous signal \( \sin \theta \) via a PLL circuit. Additionally, the DC-link voltage is maintained by supplying a real part of compensation current \( |I_r| \) via a P-I controller, as shown in (12). With the same synchronous signal \( \sin \theta \), the instantaneous current for active power balance is also yielded. Combining the above two currents generates the needed three-phase current command signals for the DSTATCOM. The paper employs a current-regulated PWM (CRPWM) inverter as the power stage of the proposed DSTATCOM. The CRPWM inverter uses the error signals from the comparison results of the reference signals and the actual compensation currents as the input. This generates the needed compensation current of the DSTATCOM for fast load compensation.

3. DSTATCOM FOR COMPENSATING AC AND DC LOADS

Various VSI topologies are described in the literature for realizing DSTATCOM to compensate unbalanced and nonlinear loads. Due to the simplicity, the absence of unbalance in the dc-link voltage and independent current tracking with respect to other phases, a three-phase H-bridge VSI topology is chosen. Figure shows a three-phase, four-wire-compensated system using an H-bridge VSI topology-based DSTATCOM compensating unbalanced and nonlinear ac load.

![Fig 3.1 Three-phase, four-wire compensated system using the H-bridge VSI topology-based DSTATCOM.]

In addition to this, a dc load \( (R_{dc}) \) is connected across the dc link. The DSTATCOM consists of 12 insulated-gate bipolar transistor (IGBT) switches each with an antiparallel diode, dc storage capacitor, three isolation transformers, and three interface inductors. The star point of the isolation transformers \( (n') \) is
connected to the neutral of load (n) and source (N). The H bridge VSIIs are connected to the PCC through interface inductors. The isolation transformers prevent a short circuit of the dc capacitor for various combinations of the switching states of the VSI. The inductance and resistance of the isolation transformers are also included in $L_f$ and $R_f$. The source voltages are assumed to be balanced and sinusoidal.

With the supply being considered as a stiff source, the feeder impedance $(L_a-R_a)$ shown in Fig. is negligible and, hence, it is not accounted in state-space modeling. To track the desired compensator currents, the VSIIs operate under the hysteresis band current control mode due to their simplicity, fast response, and being independent of the load parameters. The DSTATCOM injects currents into the PCC in such a way as to cancel unbalance and harmonics in the load currents. The VSI operation is supported by the dc storage capacitor $C_{dc}$ with voltage $v_{dc}$ across it. The dc bus voltage has two functions, that is, to support the compensator operation and to supply dc load. While compensating, the DSTATCOM maintains the balanced sinusoidal source currents with unity power factor and supplies the dc load through its dc bus.

### 3.1 State-Space Model Of The Dstatcom

For the DSTATCOM topology shown in Fig.3.1, the pairs of switches $S_{1a}-S_{2a}$ and $S_{4a}-S_{3a}$ are always ON and OFF in complimentary mode. The ON and OFF states of these switches are represented by a binary logic variable $S_a$ and its complement $\bar{S}_a$. Thus, when switches $S_{1a}-S_{2a}$ are ON, it implies that switches $S_{4a}-S_{3a}$ are OFF. This is represented by $S_a = 1$, $\bar{S}_a = 0$, and vice versa. In a similar way, $S_b$, $\bar{S}_b$, $S_c$ and $\bar{S}_c$ represent gating signals for switches $S_{1b}-S_{2b}$, $S_{4b}-S_{3b}$, $S_{1c}-S_{2c}$, and $S_{4c}-S_{3c}$, respectively. Using these notations for the system shown in Fig., the state-space equations are written as follows:

$$\dot{x} = Ax + Bu$$

where state vector $x$ and $u$ input vector are given by

$$x = [i_{fa} \ i_{fb} \ i_{fc} \ v_{dc}]^T$$

$$u = [v_{ma} \ v_{mb} \ v_{mc}]^T$$

where the superscript stands $\Gamma$ for the transpose operator. System matrix $(A)$ and $(B)$ input matrix are given as follows:

$$A = \begin{bmatrix}
-\frac{2}{L_f} & 0 & 0 & 0 \\
0 & -\frac{2}{L_f} & 0 & 0 \\
0 & 0 & -\frac{2}{L_f} & 0 \\
0 & 0 & 0 & -\frac{2}{L_f}
\end{bmatrix}$$

$$B = \begin{bmatrix}
\frac{1}{C_{dc}} & 0 & 0 & 0 \\
0 & \frac{1}{C_{dc}} & 0 & 0 \\
0 & 0 & \frac{1}{C_{dc}} & 0 \\
0 & 0 & 0 & \frac{1}{C_{dc}}
\end{bmatrix}$$

Using the above state-space model, the system state variables $(x)$ are computed at every instant.

### 3.2 Dc-Link Voltage Controllers

As mentioned before, the source supplies an unbalanced nonlinear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in Fig. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc-link voltage, closed-loop controllers are used. The proportional- integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as $K_p$, $K_i$, and $K_d$ are proportional, integral, and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain $(K_p)$ reduces rise time and steady-state error but increases the overshoot and settling time. An increase in integral gain $(K_i)$ reduces steady state error but increases overshoot and settling time. Increasing derivative gain $(K_d)$ will lead to improved stability. However, practitioners have often found that the derivative term can behave against anticipatory action in case of transport delay. A cumbersome trial-and-error method to
tune its parameters made many practitioners switch off or even exclude the derivative term. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following subsections.

3.2.1 Conventional DC-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in Fig.3.2

![Fig.3.2 Schematic diagram of the conventional dc-link voltage controller.](image)

To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the difference between the actual and reference voltages. The power required by the capacitor can be expressed as follows:

\[ P_{dc} = K_p (V_{dc,ref} - v_{dc}) + K_i \int (V_{dc,ref} - v_{dc}) dt. \]

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase supply voltage. The sampling can also be performed at a quarter cycle depending upon the symmetry of the dc-link voltage waveform. The drawback of this conventional controller is that its transient response is slow, especially for fast-changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and, hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of \( K_p \) and \( K_i \) when \( P_{dc} \) is comparable to \( P_{avg} \).

3.2.2 Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc-link capacitor \( W_{dc} \) to charge from actual voltage \( v_{dc} \) to the reference value \( V_{dc,ref} \) can be computed as

\[ W_{dc} = \frac{1}{2} C_{dc} \left( V_{dc,ref}^2 - v_{dc}^2 \right). \]

In general, the dc-link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc power \( P_{dc}' \) required by the dc-link capacitor is given as

\[ P_{dc}' = \frac{W_{dc}}{T_c} = \frac{1}{2 T_c} C_{dc} \left( V_{dc,ref}^2 - v_{dc}^2 \right) \]

where \( T_c \) is the ripple period of the dc-link capacitor voltage. Some control schemes have been reported. However, due to the lack of integral term, there is a steady-state error while compensating the combined ac and dc loads. This is eliminated by including an integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages.

![Fig.3.3 Schematic diagram of the fast-acting dc-link voltage controller.](image)

This controller is shown in Fig 6.3 and the total dc power required by the dc-link capacitor is computed as follows:

\[ P_{dc} = K_{pe} (V_{dc,ref}^2 - v_{dc}^2) + K_{ie} \int (V_{dc,ref}^2 - v_{dc}^2) dt. \]

The coefficients \( K_{pe} \) and \( K_{ie} \) are the proportional and integral gains of the proposed energy-based dc-link voltage controller. As an energy-based controller, it gives fast response compared to the conventional PI controller. Thus, it can be called a fast acting dc-link voltage controller. The ease in the calculation of the proportional and integral gains is an additional advantage. The value of the proportional controller gain \( K_{pe1} \) can be given as

\[ K_{pe1} = \frac{C_{dc}}{2 T_c}. \]

For example, if the value of dc-link capacitor is 2200 µF and the capacitor voltage ripple period as 0.01 s, then \( K_{pe1} \) is computed as 0.11. The
selection of $K_{ie}$ depends upon the tradeoff between the transient response and overshoot in the compensated source current. Once this proportional gain is selected, integral gain is tuned around and chosen to be 0.5. It is found that if $K_{ie}$ is greater than $K_{pe}/2$, the response tends to be oscillatory and if $K_{ie}$ is less than $K_{pe}/2$, then response tends to be sluggish. Hence, $K_{pe}$ is chosen to be $K_{pe}/2$.

3.3 Design Of Conventional Controller Based On The Fast-Acting Dc-Link Voltage Controller

The conventional dc-link voltage controller can be designed based on equations given for the fast-acting dc-link voltage controller and can be written as

$$P_{dc} = K_{pe}(V_{dref} - v_{dc}) + K_{ie}(V_{dref} - v_{dc})dt.$$ 

It can be also written as

$$P_{dc} = K'_{pe}(V_{dref} - v_{dc}) + K'_{ie}(V_{dref} - v_{dc})dt.$$ 

Where

$$K'_{pe} = K_{pe}(V_{dref} + v_{dc}), 
K'_{ie} = K_{ie}(V_{dref} + v_{dc}).$$

It is observed from the aforementioned equations that the gains of proportional and integral controllers vary with respect to time. However, for small ripples in the dc-link voltage, $v_{dc} \approx V_{dref}$, therefore, we can approximate the above gains to the following:

$$K'_{pe} = 2K_{pe}V_{dref}, 
K'_{ie} = 2K_{ie}V_{dref}.$$ 

The relations give approximate gains for a conventional PI controller. This is due to the fact that $V_{dref} + v_{dc}$ is not really equal to $2V_{dref}$ until variation in $v_{dc}$ is small during transients. Hence, the designed conventional PI controller works only on approximation. The open-loop gains for the two cases are given by

$$\frac{P_{dc}}{E_{ref}} = K_{pe}\left(\frac{\pi + K_{ie}}{K_{pe}}\right)$$

where $E_{ref} = V_{dref} - v_{dc}$ and

$$\frac{P_{dc}}{E_{ref}} = K'_{pe}\left(\frac{\pi + K'_{ie}}{K'_{pe}}\right).$$

Where $E_{ref} = V_{dref} - v_{dc}$. Since $K'_{pe}/K_{pe}$ is the same as $K_{ie}/K_{pe}$, the higher gain in the conventional PI controller renders less stability than that of the proposed energy-based dc-link controller. For nearly the same performance, the conventional PI controller has gains which are 364 (40/0.11 from Table) times larger than that of that proposed one. Also, the amplifier units used to realize these gains need more design considerations and are likely to saturate when used with higher gains.

### TABLE: SIMULATION PARAMETERS

<table>
<thead>
<tr>
<th>System Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>supply voltage</td>
<td>400 V (L-L), 50 Hz</td>
</tr>
<tr>
<td>Unbalanced load</td>
<td>$Z_u = 25 \Omega, Z_o = 44 + j25.5 \Omega$ and $Z = 50 + j86.6 \Omega$</td>
</tr>
<tr>
<td>Nonlinear load</td>
<td>Three-phase full wave rectifier (5 A)</td>
</tr>
<tr>
<td>DC load</td>
<td>$R_a = 100 \Omega$</td>
</tr>
<tr>
<td>DC capacitor</td>
<td>$C_p = 2000 \mu F$</td>
</tr>
<tr>
<td>Interface inductor</td>
<td>$L_i = 26 \text{ mH, } R_i = 0.25 \Omega$</td>
</tr>
<tr>
<td>Reference dc link voltage</td>
<td>$V_{dref} = 520 V$</td>
</tr>
<tr>
<td>Hysteresis band</td>
<td>$sh = 1.0 \text{ A}$</td>
</tr>
<tr>
<td>Gains of conventional dc-link voltage controller</td>
<td>$K_{pe} = 40$, $K_{ie} = 20$</td>
</tr>
<tr>
<td>Gains of fast acting dc-link voltage controller</td>
<td>$K_{pe} = 0.11$, $K_{ie} = 0.055$</td>
</tr>
</tbody>
</table>

3.4 Selection Of The Dc-Link Capacitor

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in first figure is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by $X*1000J/s$. Let us further assume that the compensator deals with half (i.e., $X/2$) and twice (i.e., $2X$) capacity under the transient conditions for n cycles with the system voltage period of $T_s$. Then, the change in energy to be dealt with by the dc capacitor is given as

$$\Delta E = (2X - X/2)nT_s.$$ 

Now this change in energy should be supported by the energy stored in the dc
capacitor. Let us allow the dc capacitor to change its total dc-link voltage from $1.4 V_m$ to $1.8 V_m$ during the transient conditions where $V_m$ is the peak value of phase voltage. Hence, we can write

$$\frac{1}{2} C_{dc} [(1.8 V_m)^2 - (1.4 V_m)^2] = (2X - X/2)nT$$

which implies that

$$C_{dc} = \frac{3XnT}{(1.8 V_m)^2 - (1.4 V_m)^2}.$$

For example, consider a 10-kVA system (i.e., $X=10$ kVA), system peak voltage $V_m = 325.2$ V, $n=0.5$, and $T=0.02$ s. The value of $C_{dc}$ computed using (23) is 2216 µF. Practically, 2000 µF is readily available and the same value has been taken for simulation and experimental studies.

4. SIMULATION STUDIES

The load compensator with H-bridge VSI topology as shown in Fig 4.1 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the PCC. The ac load consists of a three-phase unbalanced load and a three-phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance $R_{dc}$ as shown in the figure. The dc load forms 50% of the total power requirement. The system and compensator parameters are given in Table.

By monitoring the load currents and PCC voltages, the average load power is computed. At every zero crossing of phase a voltage, $I_{dc}$ is generated by using the dc-link voltage controller. The state-space equations are solved to compute the actual compensator currents and dc-link voltage. These actual currents are compared with the reference currents given by using hysteresis current control. Based on the comparison, switching signals are generated to compute the actual state variables by solving the state-space model. The source voltages and load currents are plotted in Fig 4.1(a) and (b).

The load currents have total harmonic distortions of 8.9%, 14.3%, and 21.5% in phases a, b and c, respectively. The unbalance in load currents results in neutral current as illustrated in the figure. The compensator currents and compensated source currents are shown in Fig.4.1 (c) and (d). As seen from Fig. 4.1(d), the source currents are balanced sinusoids; however, the switching frequency components are superimposed over the reference currents due to the switching action of the VSI. The currents have a unity power factor relationship with the voltages in the respective phases. The THDs in these currents are 3.6%, 3.7%, and 3.9% in phases a, b and c, respectively.
There are notches in the source currents due to finite bandwidth of the VSI. The transient performance of the conventional and fast-acting dc-link voltage controllers are studied by making sudden changes in the ac load supplied by the ac load bus as well as the dc load supplied by the dc link. In the simulation study, the load is halved at the instant $t=0.4$ s and brought back to full load at $t=0.8$ s. The transient performance is explained in the following subsections.

**CONCLUSION**

A VSI topology for DSTATCOM compensating ac unbalanced and nonlinear loads and a dc load supplied by the dc link of the compensator is presented. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. An energy-based fast-acting dc-link voltage controller is suggested to ensure the fast transient response of the compensator. Mathematical equations are developed to compute the gains of this controller. The efficacy of the proposed controller over the conventional dc-link voltage controller is established through the digital simulation and experimental studies. It is observed from these studies that the proposed dc-link voltage controller gives fast transient response under load transients.

**REFERENCES**


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Multilevel Converters Based on VSC on Railway Electrification System

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Abstract:-This paper proposes a new railway electrification system in which the voltage-source converter (VSC) becomes the basic building block. This will allow existing railways, comprising several ac and dc subsystems, to be transformed into simpler medium-voltage dc (MVDC) multi terminal power systems feeding mobile loads. Moreover, the VSC-based unified scheme will substantially facilitate the connectivity among otherwise heterogeneous railway systems, while the integration of distributed generation and storage is achieved in a straightforward fashion. In addition to the general MVDC architecture, details are provided about the dc catenary layout, dual-voltage locomotive configurations, and dc-dc links between urban and long-distance railways. The need for a supervisory control system, and its role in coordinating local VSC controllers, so that the resulting power flows are optimized while the catenary voltage is kept within limits, are discussed. The proposed railway electrification paradigm is compared with the standard 25-kv, ac electrification system by means of a real.

1. INTRODUCTION

The static synchronous compensator (STATCOM) has been well accepted as a power system controller for improving voltage regulation and reactive compensation [1]–[5]. There are several compelling reasons to consider a multilevel converter topology for the STATCOM [6]–[8]. These well known reasons include the following: 1) lower harmonic injection into the power system; 2) decreased stress on the electronic components due to decreased voltages; and 3) lower switching Losses [9]. Various multilevel converters also readily lend themselves to a variety of PWM strategies to improve efficiency and control. An eleven-level cascaded multilevel STATCOM is shown in Fig. 1.1. This converter uses several full bridges in series to synthesize staircase waveforms. Because every full bridge can have three output voltages with different switching combinations, the number of output voltage levels is $2^n + 1$ where $n$ is the number of full bridges in every phase. The converter cells are identical and therefore modular. As higher level converters are used for high output rating power applications, a large number of power switching devices will be used. Each of these devices is a potential failure point. Therefore, it is important to design a sophisticated control to produce a fault-tolerant STATCOM. A faulty power cell in a cascaded H-Bridge STATCOM can potentially cause switch modules to explode leading to the fault conditions such as a short circuit or an overvoltage on the power system resulting in an expensive down time.

Subsequently, it is crucial to identify the existence and location of the fault for it to be removed. Several fault detection methods have been proposed over the last...
few years. Resistor sensing, current transformation, and VCE sensing are some of the more common approaches. For example, a method based on the output current behavior is used to identify IGBT short circuits [12]. The primary drawback with the proposed approach is that the fault detection time depends on the time constant of the load. Therefore, for loads with a large $RL$ time constant, the faulty power cell can go undetected for numerous cycles, potentially leading to circuit damage. Another fault detection approach proposed in [13] is based on a switching frequency analysis of the output phase voltage. This method was applied to flying capacitor converters and has not been extended to cascaded converters. AI-based methods were proposed to extract pertinent signal features to detect faults in [14]. In [15], sensors are used to measure each IGBT current and to initiate switching if a fault is detected. A fault-tolerant neutral point-clamped converter was proposed, a reconfiguration system based on bidirectional switches has been designed for three-phase asymmetric cascaded H-bridge inverters. The fundamental output voltage phase shifts are used to rebalance a faulted multilevel cascaded converter in [18].

Fig 1.1. Eleven-level cascaded VSC-based MVDC Railway Electrification System.

In this paper, the method we propose requires only that the output dc link voltage of each phase be measured. This measurement is typically accomplished anyway for control purposes. If a fault is detected, the module in which the fault occurred is then isolated and removed from service. This approach is consistent with the modular design of cascaded converters in which the cells are designed to be interchangeable and rapidly removed and replaced. Until the module is replaced, the multilevel STATCOM continues to operate with slightly decreased, but still acceptable, performance.

In summary, this approach offers the following advantages:
- No additional sensing requirements;
- Additional hardware is limited to two bypass switches per module;
- Is consistent with the modular approach of cascaded multilevel converters; and
- The dynamic performance and THD of the STATCOM is not significantly impacted.

2. FACTS DEVICES

The power system is an interconnection of generating units to load centers through high voltage electric transmission lines and in general is mechanically controlled. It can be divided into three subsystems: generation, transmission and distribution subsystems. Until recently all three subsystems were under supervision of one body within a certain geographical area providing power at regulated rates. In order to provide cheaper electricity the deregulation of power system, which includes separate generation, Transmission and distribution companies, is already being implemented. At the same time electric power demand continues to grow and also building of the new generating units and transmission circuits is becoming more difficult because of economic and environmental reasons.
Therefore, power utilities are forced to rely on utilization of existing generating units and to load existing transmission lines close to their thermal limits. However, stability has to be maintained at all times. Hence, it is necessary to operate power system effectively, without reduction in the systems security and quality of supply, even in the case of contingency conditions. The contingency may be such as loss of transmission lines and/or generating units, which occur frequently, and will most probably occur at higher frequencies. So a new control strategies need to be implemented, to take care of such expected situations.

Flexible AC Transmission Systems (FACTS) technology is based on the use of power electronic controlled devices for allowing transmission circuits to be used to their maximum thermal capability. In particular the FACTS devices aim principally to control the three main parameters directly effecting AC power transmission namely voltage, phase angle, and impedance. High Voltage Direct Current (HVDC) transmission is parallel technology using power electronics and is not normally included as a FACTS technology. FACTS controllers can be broadly divided into four categories, which are

- Series controllers
- Shunt controllers
- Combined Series-Series Controllers
- Combined Series -Shunt controllers

3. HARMONIC

The typical definition for a harmonic is “a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency.” [1]. Some references refer to “clean” or “pure” power as those without any harmonics. But such clean waveforms typically only exist in a laboratory. Harmonics have been around for a long time and will continue to do so. In fact, musicians have been aware of such since the invention of the first string or woodwind instrument. Harmonics (called “overtones” in music) are responsible for what makes a trumpet sound like a trumpet, and a clarinet like a clarinet.

Electrical generators try to produce electric power where the voltage waveform has only one frequency associated with it, the fundamental frequency. In the North America, this frequency is 60 Hz, or cycles per second. In European countries and other parts of the world, this frequency is usually 50 Hz. Aircraft often uses 400 Hz as the fundamental frequency. At 60 Hz, this means that sixty times a second, the voltage waveform increases to a maximum positive value, then decreases to zero, further decreasing to a maximum negative value, and then back to zero. The rate at which these changes occur is the trigometric function called a sine wave, as shown in figure 1. This function occurs in many natural phenomena, such as the speed of a pendulum as it swings back and forth, or the way a string on a violin vibrates when plucked.
50Hz, the second harmonic is 2*50 or 100Hz.

300Hz is the 5th harmonic in a 60 Hz system, or the 6th harmonic in a 50 Hz system. Figure 2 shows how a signal with two harmonics would appear on an oscilloscope-type display, which some power quality analyzers provide.

Figure 2 shows how a signal with two harmonics would appear on an oscilloscope-type display, which some power quality analyzers provide.

In order to be able to analyze complex signals that have many different frequencies present, a number of mathematical methods were developed. One of the more popular is called the Fourier Transform. However, duplicating the mathematical steps required in a microprocessor or computer-based instrument is quite difficult. So more compatible processes, called the FFT for Fast Fourier transform, or DFT for Discrete Fourier Transform, are used.

4. MULTILEVEL INVERTER

In response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter.

As reported in the literature, the H-bridge cascade inverter has been used in several practical instances for broadcasting amplifier, plasma, industrial drive as well as STATCOM applications etc. The main limitation of the H-bridge cascade inverter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. For STATCOM application, where the isolated supplies are not required, the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates over-sizing of the dc link capacitors.

The capacitor clamping inverter, though the three-level scheme of which was published in the early 1980’s [8], had been rarely discussed until the introduction of the “imbricated cells” [9]. The individual clamping capacitor needs only to smooth the switching frequency ripple voltage and the required capacity for each clamping capacitor is therefore small. However, as the number of level increases, such problems as thermal designing, low-inductance designing, as well as insulation designing of the system will become critical. Medium voltage drives using four-level capacitor clamping inverter has recently been available on the market.

5. MULTILEVEL STATCOM

5.1 Introduction

A cascaded multilevel STATCOM contains several H-bridges in series to synthesize a staircase waveform. The inverter legs are identical and are therefore modular. In the eleven-level STATCOM, each leg has five H-bridges. Since each full bridge generates three different level voltages \( V, 0, -V \) under different switching states, the number of output voltage levels will be eleven. A multilevel
configuration offers several advantages over other converter types [19].

1) It is better suited for high-voltage, high-power applications than the conventional converters since the currents and voltages across the individual switching devices are smaller.

2) It generates a multistep staircase voltage waveform approaching a more sinusoidal output voltage by increasing the number of levels.

3) It has better dc voltage balancing, since each bridge has its own dc source.

To achieve a high-quality output voltage waveform, the voltages across all of the dc capacitors should maintain a constant value. Variations in load cause the dc capacitors to charge and discharge unevenly leading to different voltages in each leg of each phase. However, because of the redundancy in switching states, there is frequently more than one state that can synthesize any given voltage level. Therefore, there exists a “best” state among all the possible states that produces the most balanced voltages [20]. Since there are multiple possible switching states that can be used to synthesize a given voltage level, the particular switching topology is chosen such that the capacitors with the lowest voltages are charged or conversely, the capacitors with the highest voltages are discharged. This redundant state selection approach is used to maintain the total dc link voltage to a near constant value and each individual cell capacitor within a tight bound. Different pulse width modulation (PWM) techniques have been used to obtain the multilevel converter output voltage. One common PWM approach is the phase shift PWM (PSPWM) switching concept [21].

The PSPWM strategy causes cancellation of all carrier and associated sideband harmonics up to the \((N - 1)\)th carrier group for an \(N\)-level converter. Each carrier signal is phase shifted by

\[
\phi = \frac{2\pi}{N}
\]

Fig. 5.1. (a) Carrier and reference waveform for PSPWM. (b) Output waveform.

Fig. 5.2. Cell with fault switch.

Where \(n\) is the number of cells in each phase. Fig. 2 illustrates the carrier and reference waveforms for a phase leg of the eleven-level STATCOM. In this figure, the carrier frequency has been decreased for better clarity. Normally, the carrier frequency for PWM is in the range of 1–10 khz.

6.2 Fault Analysis for the Multilevel Statcom

A converter cell block, as shown in Fig. 5.2, can experience several types of faults. Each switch in the cell can fail in an open or closed state. The closed state is the most severe failure since it may lead to
shoot through and short circuit the entire cell. An open circuit can be avoided by using a proper gate circuit to control the gate current of the switch during the failure [23]. If a short circuit failure occurs, the capacitors will rapidly discharge through the conducting switch pair if no protective action is taken. Hence, the counterpart switch to the failed switch must be quickly turned off to avoid system collapse due to a sharp current surge. Nomenclature for the proposed method is given in Table I.

![Table I: Nomenclature](image)

Fig. 5.3. Simplified eleven-level cascaded multilevel STATCOM.

The staircase voltage waveform shown in Fig. 5.1 is synthesized by combining the voltages of the various cells into the desired level of output voltage. At the middle levels of the voltage waveform, due to the switching state redundancy, there are more than one set of switching combinations that may be used to construct the desired voltage level. Therefore, by varying the switching patterns, the loss of any individual cell will not significantly impact the middle voltages of the output voltage. However, the peak voltages require that all cells contribute to the voltage; therefore, the short circuit failure of any one cell will lead to the loss of the first and \((2n + 1)\) output levels and cause degradation in the ability of the STATCOM to produce the full output voltage level. Consider the simplified eleven-level converter shown in Fig. 5.3. The process for identifying and removing the faulty cell block is summarized in Fig. 5.4. The input to the detection algorithm is \(\hat{E}_{\text{out}}\) for each phase, where \(\hat{E}_{\text{out}}\) is the STATCOM RMS output voltage. If the STATCOM RMS output voltage drops below a preset threshold value \(E_\text{th}\), then, a fault is known to have occurred (see Fig. 5.5). Once a fault has been detected to have occurred, then, the next step is to identify the faulty cell. By utilizing the switching signals in each converter cell, (i.e., \(S_1\) and \(S_2\)), it is possible to calculate all of the possible voltages that can be produced at any given instant as illustrated in Table II (terminology adopted from... Thus, the output voltage of a cell is

\[
v_{ax} = v_{az} + v_{\alpha x}
\]

And since the cells of the STATCOM are serially connected, the total output voltage per phase is

\[
v_{y0} = \sum_{y=1}^{n} v_{y}\quad,\quad y \in \{a, b, c\}
\]

where \(n\) is the number of blocks.

![Diagram 5.4: Fault Identification Process](image)
Fig. 5.4. Eleven-level converter VSC Based MVDC Railway Electrification System.

Fig. 5.5. VSC-Based MVDC Railway - filtered output voltage and threshold value.

By utilizing the switching signals in each converter cell, (i.e., $S_j1$ and $S_j2$, $j$ is the cell number), it is possible to calculate all of the possible voltages that can be produced at any given instant. When there is a fault in the multilevel converter, the capacitor at the faulty block will rapidly discharge. This discharge results in a phase shift in the output ac voltage as well as a change in amplitude of voltage. The set of all possible phase fault voltages for an eleven-level converter is given by

$$f_i = V_{dc0}(S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2})$$

(cell 1 faulted)

$$f_2 = V_{dc0}(S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2})$$

(cell 2 faulted)

$$\vdots$$

$$f_5 = V_{dc0}(S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2} + S_{i1} - S_{i2})$$

(cell 5 faulted)

or more succinctly as

$$f_i = V_{dc0} \sum_{j=1}^{n} (S_{j1} - S_{j2}), \quad i = 1, \ldots, n \quad (3)$$

### Table II

**Switching State and Output Voltage of an H-Bridge**

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$v_{DC}$</th>
<th>$v_{PE}$</th>
<th>$v_{PC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-v_{DC}</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$v_{DC}$</td>
<td>0</td>
<td>$v_{PE}$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$v_{PC}$</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig: 6.1 Circuit diagram

Fig: 6.2 Pulse generator

Fig: 6.3 Controller
In this project, a fault detection and mitigation strategy for a multilevel cascaded converter has been proposed. This approach requires no extra sensors and only one additional bypass switch per module per phase. The approach has been validated on a 115-kv system with a STATCOM compensating an electric arc furnace load. This application was chosen since the arc furnace provides a severe application with its non sinusoidal, unbalanced, and randomly fluctuating load. The proposed approach was able to accurately identify and remove the faulted module. In addition, the STATCOM was able to remain in service.
and continue to provide compensation without exceeding the total harmonic distortion allowances.

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Speed Control of BLDC Motor Drive by Using Buck–Boost Converter

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Abstract: This kind of papers provides an power factor corrected (PFC) bridgeless (BL) buck–boost converter-fed brushless direct current (BLDC) motor as a cost-effective alternative pertaining to low-power apps. A technique of pace handle on the BLDC motor by managing the particular dc link voltage on the voltage source inverter (VSI) is employed with a sole voltage sensor. This kind of allows for the particular operation of VSI on essential volume moving over using the electric commutation on the BLDC motor that offers reduced moving over loss. The BL setting on the buck–boost converter is actually offered that offers the particular reduction on the diode fill rectifier, hence decreasing the particular conduction loss linked to it. The PFC BL buck–boost converter was designed to work throughout discontinuous inductor recent function (DICM) to provide the natural PFC on ac mains. This functionality on the offered get is actually examined on the wide range of pace handle and different present voltages (universal ac mains on 90–265 V) with improved energy quality on ac mains. This acquired energy quality indices usually are from the satisfactory restricts of worldwide energy quality requirements for example the IEC 61000-3-2. This functionality on the offered get is actually simulated throughout MATLAB/Simulink surroundings, plus the acquired email address particulars are endorsed experimentally over a formulated prototype on the get.

1 Introduction
Permanent magnet brushless DC motors (PMBLDCMs) are preferred motors for a compressor of an air-conditioning (Air-Con) system due to its features like high efficiency, wide speed range and low maintenance requirements. The operation of the compressor with the speed control results in an improved efficiency of the system while maintaining the temperature in the air-conditioned zone at the set reference consistently. Whereas, the existing air conditioners mostly have a single-phase induction motor to drive the compressor in ‘on/off’ control mode. This results in increased losses due to frequent ‘on/off’ operation with increased mechanical and electrical stresses on the motor, thereby poor efficiency and reduced life of the motor.

Moreover, the temperature of the air conditioned zone is regulated in a hysteresis band. Therefore, improved efficiency of the Air-Con system will certainly reduce the cost of living and energy demand to cope-up with ever-increasing power crisis. A PMBLDCM which is a kind of three-phase synchronous motor with permanent magnets (PMs) on the rotor and trapezoidal back EMF waveform operates on electronic commutation accomplished by solid state switches. It is powered through a three-phase voltage source inverter (VSI) which is fed from single-phase AC supply using a diode bridge rectifier (DBR) followed by smoothening DC link capacitor. The compressor exerts constant torque (i.e. rated torque) on the PMBLDCM and is operated in speed control mode to improve the efficiency of the Air-Con system.

Since, the back-emf of the PMBLDCM is proportional to the motor speed and the developed torque is proportional to its phase current, therefore, a constant torque is maintained by a constant current in the stator winding of the PMBLDC motor whereas the speed can be controlled by varying the terminal voltage of the motor. Based on this logic, a speed control scheme is proposed in this paper which uses a reference voltage at DC link proportional to the desired speed of the PMBLDC motor. However, the control of VSI is only for electronic commutation which is based on the rotor position signals of the PMBLDC motor.

The PMBLDCM drive, fed from a single-phase AC mains through a diode bridge rectifier (DBR) followed by a DC link capacitor, suffers from power quality (PQ) disturbances such as poor power factor (PF), increased total harmonic distortion (THD) of current at input AC mains and its high crest factor (CF). It is mainly due to uncontrolled charging of the DC link capacitor which results in a pulsed current waveform having a peak value higher than the amplitude of the fundamental input current at AC...
mains. Moreover, the PQ standards for low power equipments emphasize on low harmonic contents and near unity power factor current to be drawn from AC mains by these motors.

The proposed PMBLDCM drive is modeled in Mat lab-Simulink environment and evaluated for an air conditioning compressor load. The compressor load is considered as a constant torque load equal to rated torque with the speed control required by air conditioning system. A 1.5 kW rating PMBLDCM is used to drive the air conditioner compressor, speed of which is controlled effectively by controlling the DC link voltage. The detailed data of the motor and simulation parameters are given in Appendix. The performance of the proposed PFC drive is evaluated on the basis of various parameters such as total harmonic distortion (THDi) and the crest factor (CF) of the current at input AC mains, displacement power factor (DPF), power factor (PF) and efficiency of the drive system (ηdrive) at different speeds of the motor. Moreover, these parameters are also evaluated for variable input AC voltage at DC link voltage of 416 V which is equivalent to the rated speed (1500 rpm) of the PMBLDCM.

2. Power Factor Correction (PFC)

An electric utility's power load on an electrical distribution system fall into one of three categories; resistive, inductive or capacitive. In most industrial facilities, the most common power usages are "inductive." Examples of inductive loads include transformers, fluorescent lighting and AC induction motors. Most inductive loads use a conductive coil winding to produce an electromagnetic field which permits the motor to function. All inductive loads require two different types of power for the motor to operate: Active power (measured in kW or kilowatts) - this power produces the motive force Reactive power (kvar) - this energizes the magnetic field of the motor. The operating power from the distribution system is composed of both active (working) and reactive (non-working) elements. The active power does useful work in driving the motor whereas the reactive power only provides the magnetic field. Unfortunately, electric utility's customers are charged for both active and reactive power. Example: A customer's power factor drops, the system becomes less efficient.

A drop from 1.0 to 0.9 results in 15% more current being required for the same load. A power factor of 0.7 requires approximately 40% more current; and a power factor of 0.5 requires approximately 100% (twice as much) to handle the same load. The answer to these problems is to reduce the reactive power drawn from the supply by improving the power factor. If an AC motor were 100% efficient it would consume only active power. However, since most AC motors are only 75% to 80% efficient, they operate at a lower power factor. This means inefficient and even "wasteful" energy usage and cost efficiency because most electric utilities charge penalties for poor, inefficient power factor. Simply installing capacitors will improve a commercial or industrial company's power factor and will result in savings on their electricity bill every month. An additional potential benefit for correcting poor power factor includes. Reduction of heating losses in transformers and distribution equipment Longer equipment life

2.1. BLDC motors

BLDC motors find applications in every segment of the market. Automotive, appliance, industrial controls, automation, aviation and so on, have applications for BLDC motors. Out of these, we can categorize the type of BLDC motor control into three major types

- Constant load
- Varying loads
- Positioning applications

3. INVERTER OPERATION

Inverter is power electronic circuit that converts a direct current into an alternative current power of desired magnitude and frequency with the use of appropriate transformers, switching and control circuits. The inverters find their application in modern ac motor and uninterruptible power supplies. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC. The inverter performs the opposite function of a rectifier.

3.2 Classification of Inverter

a) Based on the source used

- Voltage source inverter
- Current source inverter
b) Based on switching methods
- Pulse width modulation inverters
- Square wave inverters
c) Based on switching devices used
- Transistorized inverter
- Thyristorized inverter
d) Based on the inversion principle
- Resonant inverter
- Non-Resonant inverter

4. Proposed Speed Control Scheme of PMBLDC Motor for Air Conditioner

The proposed speed control scheme (as shown in Fig. 4.1) controls reference voltage at DC link as an equivalent reference speed, thereby replacing the conventional control of the motor speed and a stator current involving various sensors for voltage and current signals. Moreover, the rotor position signals are used to generate the switching sequence for the VSI as an electronic commutator of the PMBLDC motor. Therefore, rotor-position information is required only at the commutation points, e.g., every 60°electrical in the three phase. The rotor position of PMBLDCM is sensed using hall effect position sensors and used to generate switching sequence for the VSI as shown in Table-I.

The DC link voltage is controlled by a half-bridge buck DC-DC converter based on the duty ratio (D) of the converter. For a fast and effective control with reduced size of magnetic and filters, a high switching frequency is used; however, the switching frequency (fs) is limited by the switching device used, operating power level and switching losses of the device. Metal oxide field effect transistors (MOSFETs) are used as the switching device for high switching frequency in the proposed PFC converter. However, insulated gate bipolar transistors (IGBTs) are used in VSI bridge feeding PMBLDCM, to reduce the switching stress, as it operates at lower frequency compared to PFC switches. The PFC control scheme uses a current control loop inside the speed control loop with current multiplier approach which operates in continuous conduction mode (CCM) with average current control. The control loop begins with the comparison of sensed DC link voltage with a voltage equivalent to the reference speed. The resultant voltage error is passed through a proportional-integral (PI) controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and compared with DC current sensed after the DBR.

The resultant current error is amplified and compared with saw-tooth carrier wave of fixed frequency (fs) in unipolar scheme (as shown in Fig. 4.2) to generate the PWM pulses for the half-bridge converter. For the current control of the PMBLDCM during step change of the reference voltage due to the change in the reference speed, a voltage gradient less than 800 V/s is introduced for the change of DC link voltage, which ensures the stator current of the PMBLDCM within the specified limits (i.e. double the rated current).

Fig 4.1 Control schematic of Proposed Bridge-buck PFC converter fed PMBLDCM drive

4.2 Design of PFC Buck Half-Bridge Converter Based PMBLDCM Drive

The proposed PFC buck half-bridge converter is designed for a PMBLDCM drive with main considerations on PQ constraints at AC mains and allowable ripple in DC link voltage. The DC link voltage of the PFC converter is given as

\[ V_{dc} = 2 \left( \frac{N_2}{N_1} \right) V_{in} \text{D} \text{ and } N_2 = N_{21} = N_{22} \ldots \ldots \ldots \ldots \text{ (1)} \]

Where \( N_1, N_{21}, N_{22} \) are number of turns in primary, secondary upper and lower windings of the high frequency (HF) isolation transformer, respectively.
Vin is the average output of the DBR for a given AC input voltage (Vs) related as,

$$V_{\text{in}} = 2\sqrt{2}V_s/\pi$$  \hspace{1cm} (2)

A ripple filter is designed to reduce the ripples introduced in the output voltage due to high switching frequency for constant of the buck half-bridge converter. The inductance (Lo) of the ripple filter restricts the inductor peak to peak ripple current (ΔILo) within specified value for the given switching frequency (fs), whereas, the capacitance (Cd) is calculated for a specified ripple in the output voltage (ΔVCd). The output filter inductor and capacitor are given as,

$$L_o = (0.5-D)V_d/{f_s(\Delta I_{Lo})}$$ \hspace{1cm} (3)

$$C_d = L_o/(2\omega \Delta V_{Cd})$$ \hspace{1cm} (4)

The PFC converter is designed for a base DC link voltage of $V_{dc} = 400$ V at $V_{in} = 198$ V from $V_s = 220$ Vrms. The turn’s ratio of the high frequency transformer (N2/N1) is taken as 6:1 to maintain the desired DC link voltage at low input AC voltages typically at 170V. Other design data are $f_s = 40$ kHz, $I_o = 4$ A, $\Delta V_{Cd} = 4$ V (1% of $V_{dc}$), $\Delta I_{Lo} = 0.8$ A (20% of $I_o$). The design parameters are calculated as $L_o = 2.0$ mH, $C_d = 1600 \mu$F.

5. RESULTS AND DISCUSSIONS

5.1 Simulation Model

The performance of the proposed PMBLDCM drive fed from 220 V AC mains during starting at rated torque and 900 rpm speed is shown.
in Fig. 5.2. A rate limiter of 800 V/s is introduced in the reference voltage to limit the starting current of the motor as well as the charging current of the DC link capacitor. The PI controller closely tracks the reference speed so that the motor attains reference speed smoothly within 0.35 sec while keeping the stator current within the desired limits i.e. double the rated value. The current (is) waveform at input AC mains is in phase with the supply voltage (vs) demonstrating nearly unity power factor during the starting.

5.2.2 PMBLDCM drive under speed variation from 900 to 1500 rpm

During Transient Condition shows the performance of the drive during the speed control of the compressor. The reference speed is changed from 900 rpm to 1500 rpm for the rated load performance of the compressor; It is observed that the speed control is fast and smooth in either direction i.e. acceleration or retardation with power factor maintained at nearly unity value. Moreover, the stator current of PMBLDCM is within the allowed limit (twice the rated current) due to the introduction of a rate limiter in the reference voltage. The results are shown like voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase ‘a’ (Ia), and shaft power output (Po).

5.2.3 PMBLDCM drive under speed variation from 900 to 300 rpm

During Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for speed at 300 rpm and the results are shown like voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase ‘a’ (Ia), and shaft power output (Po).

5.2.4 Performance of the PMBLDCM drive at 300 rpm

During Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for speed at 300 rpm and the results are shown like voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase ‘a’ (Ia), and shaft power output (Po).
current of the motor for phase ‘a’ (Ia), and shaft power output (Po).

5.2.5 Performance of the PMBLDCM drive at 900 rpm

![Graph showing performance at 900 rpm]

**Fig 5.6 Performance of the PMBLDCM drive at 900 rpm**

During Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for speed at 900 rpm and the results are shown like voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase ‘a’ (Ia), and shaft power output (Po).

5.2.6 Performance of the PMBLDCM drive at 1500 rpm

![Graph showing performance at 1500 rpm]

**Fig 5.7 Performance of the PMBLDCM drive at 1500 rpm**

During Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for speed at 1500 rpm and the results are shown like voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase ‘a’ (Ia), and shaft power output (Po).

6. CONCLUSION

A new speed control strategy of a PMBLDCM drive is validated for a compressor load of an air conditioner which uses the reference speed as an equivalent reference voltage at DC link. The speed control is directly proportional to the voltage control at DC link. The rate limiter introduced in the reference voltage at DC link effectively limits the motor current within the desired value during the transient condition (starting and speed control). The additional PFC feature to the proposed drive ensures nearly unity PF in wide range of speed and input AC voltage. Moreover, power quality parameters of the proposed PMBLDCM drive are in conformity to an International standard IEC 61000-3-2. The proposed drive has demonstrated good speed control with energy efficient operation of the drive system in the wide range of speed and input AC voltage. The proposed drive has been found as a promising candidate for a PMBLDCM driving Air-Con load in 1-2 kW power range.

7. REFERENCES


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Designing of Data Matching Encoded System Low Complexity Using BWA

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Abstract:-In current scenario, there are situations in a computing system where incoming information needs to be compared with a piece of stored data to locate the matching entry, e.g., cache tag array lookup and translation look-aside buffer matching. Nowadays the reliability issues of memory are Event Upsets (EUs), which are able to invert the stored logical value in memory cells. This issue is more serious when the affected memory cells are part of the configuration memory used for programming the circuit functionality. The consequences may be alterations of the circuit functionality causing errors which may only be corrected by reprogramming the device. A new architecture for matching the data protected with an error-correcting code (ECC) is proposed in brief to reduce latency and complexity. The proposed architecture is based on the fact that the codeword of an ECC is usually represented in a systematic form consisting of the raw data and the parity information generated by encoding, and the proposed architecture parallelizes the comparison of the data and that of the parity information. To further reduce the latency and complexity, in addition, a new butterfly-formed weight accumulator (BWA) is proposed for the efficient computation of the Hamming distance. Grounded on the BWA, the proposed architecture examines whether the incoming data matches the stored data, and if not it aims to locate the erroneous bit and they are corrected. The empirical evaluation proves that the proposed methodology discovers the best service for reliability issues of memory.

I. INTRODUCTION
Data comparison circuit is a logic that has many applications in a computing system. For example, to check whether a piece of information is in a cache, the address of the information in the memory is compared to all cache tags in the same set that might contain that address. Another place that uses a data comparison circuit is in the translation look-aside buffer (TLB) unit. TLB is used to speed up virtual to physical address translation. Error correcting codes (ECCs) are widely used in modern microprocessors to enhance the reliability and data integrity of their memory structures. Several error detecting codes (EDCs) and error correcting codes (ECCs) have been proposed so far to improve cache reliability. They range from the simple parity check code to the more complex Single Error Correcting/Double Error Detecting (SEC/DED) ECC (used to protect the L2 and L3 caches in the Itanium microprocessor).

II. DATA COMPARISON METHODS
2.1 Decode-And-Compare Architecture
This describes the conventional decode-and-compare architecture. Let us consider a cache memory where a k bit tag is stored in the form of an n-bit codeword after being encoded by a (n, k) code. In the decode-and-compare architecture, the n-bit retrieved codeword should first be decoded to extract the original k-bit tag. The extracted k-bit tag is then compared with the k-bit tag field of
an incoming address to determine whether the tags are matched or not. As the retrieved codeword should go through the decoder before being compared with the incoming tag, the critical path is too long to be employed in a practical cache system designed for highspeed access.

2.2 Direct Compare Method
Direct compare method is one of the most recent solutions for the matching problem. The direct compare method encodes the incoming data and then compares it with the retrieved data that has been encoded as well. Therefore, the method eliminates the complex decoding from the critical path.

2.3 Sa-Based Approach
SA-based approach is the one where a special counter is constructed with an additional building block called saturating adder (SA). The SA-based direct compare architecture reduces the latency and hardware complexity by resolving the aforementioned drawbacks.

III. ADVANCED DATA COMPARISION METHODS
3.1 DMC Encoding
Because of high-speed caches and main memories, which are prone to soft errors, error correcting codes are used in the design and, more recently, in the design of on chip memories. For the encoding Decimal matrix code (DMC) is proposed to assure reliability in the presence of MCUs with reduced performance overheads, and a 4-bit word is encoded based on the proposed technique. First, during the encoding process, information bits i are fed to the DMC encoder, and then the horizontal redundant bits H and vertical redundant bits V are obtained from the DMC encoder. When the encoding process is completed, the obtained DMC codeword is stored in the memory.

![Fig1: XOR bank structure for (8,4) code](image)

3.3 Butterfly Formed Weight Accumulator
The proposed architecture grounded on the data path design is given below. It contains multiple butterfly formed weight accumulators (BWAs) proposed to improve the latency and complexity of the Hamming distance computation. The basic function of the BWA is to count the number of 1’s among its input bits. The proposed architecture consists of multiple stages of HAs as shown in figure where each output bit of a HA is associated with a weight. The HAs in a stage are connected in a butterfly form so as to accumulate the carry bits and the sum bits of the upper stage separately. In other words, both inputs of a HA in a stage, except the first stage, are either carry bits or sum bits computed in the upper stage. This connection method leads to a property that if an output bit of a HA is set, the number of 1’s among the bits in the paths reaching the HA is equal to the weight of the output bit.
Fig 2: General structure of BWA
In above figure for example, if the carry bit of the gray-colored HA is set, the number of 1’s among the associated input bits, i.e., A, B, C, and D, is 2. At the last stage of above figure the number of 1’s among the input bits, d, can be calculated as:

\[ d = 8I + 4(J + K + M) + 2(L + N + O) + P \]

Since what we need is not the precise Hamming distance but the range it belongs to, it is possible to simplify the circuit. When \( r_{\text{max}} = 1 \), for example, two or more than two 1’s among the input bits can be regarded as the same case that falls in the fourth range. In that case, we can replace several HAs with a simple OR-gate tree as shown below. This is an advantage over the SA that resorts to the compulsory saturation.

Fig 3: Revised structure with OR-gate tree
Each XOR stage generates the bitwise difference vector for either data bits or parity bits, and the following processing elements count the number of 1’s in the vector, i.e., the Hamming distance. Each BWA at the first level is in the revised form shown in figure above, and generates an output from the OR-gate tree and several weight bits from the HA trees. In the interconnection, such outputs are fed into their associated processing elements at the second level.

The output of the OR-gate tree is connected to the subsequent OR-gate tree at the second level, and the remaining weight bits are connected to the second level BWAs according to their weights. More precisely, the bits of weight \( w \) are connected to the BWA responsible for \( w \)-weight inputs. Each BWA at the second level is associated with a weight of a power of two that is less than or equal to \( P_{\text{max}} \), where \( P_{\text{max}} \) is the largest power.

As the weight bits associated with the fourth range are all ORed in the revised BWAs, there is no need to deal with the powers of two that are larger than \( P_{\text{max}} \). A simple \((8, 4)\) single-error correction double-error detection code is considered and the corresponding first and second level circuits are shown below.

Fig 4: First and second level circuits for \((8, 4)\) code

3.4 Decision Unit
Taking the outputs of the preceding circuits (BWA), the decision unit finally determines the incoming tag matches the retrieved codeword by considering the four ranges of the Hamming distance. The decision unit is in fact a combinational logic of which functionality is specified by a truth table that takes the outputs of the preceding circuits as inputs. For the \((8, 4)\) code that the corresponding first and second level circuits are given above, the truth table for the decision unit is described in Table I. Since \( U \) and \( V \) cannot be set simultaneously, such cases are implicitly included in do not care terms in Table I.

Table I. Truth table of the decision unit for \((8, 4)\) code

<table>
<thead>
<tr>
<th>Q OR R S</th>
<th>T</th>
<th>U</th>
<th>V</th>
<th>DECISION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>MATCH</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>FAULT</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>FAULT</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MISMATCH</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>MISMATCH</td>
<td></td>
</tr>
</tbody>
</table>
3.5 Error Deduction and Correction

Decimal error deduction technique is proposed and it has several advantages over the simple binary error deduction technique. The Limits of Simple Binary Error Detection can be given as follows:

- It requires low redundant bits; its error detection capability is limited. The main reason for this is that its error detection mechanism is based on binary.
- The number of even bit errors cannot be detected.
- Can detect only a finite number of errors finite number of errors

However, when the decimal algorithm is used to detect errors, these errors can be detected so that the decoding error can be avoided. The reason is that the operation mechanism of decimal algorithm is different from that of binary. First of all, the horizontal redundant bits H1 H0 are obtained from the original information bits. When MCUs occur in symbols, i.e., the bits in symbols are upset to “1” from “0” or vice versa.

The proposed DMC can easily correct upsets of the following types:

- Type 1 is a single error
- Type 2 is an inconsecutive error in two consecutive symbols
- Type 3 is a consecutive error in two consecutive symbols
- Type 4 is an inconsecutive error in two inconsecutive symbols
- Type 5 is a consecutive error in four consecutive symbols

IV. RESULTS

The following screenshots include power analysis report, combinational delay, device utilization summary, and the output waveform.

**CONCLUSION**

In this method, we make use of the DMC technique to assure the reliability of memory. The proposed protection code utilizes decimal algorithm to detect errors, so that more errors were detected and corrected. To reduce the hardware complexity and latency, a new architecture has been presented for matching the data protected with an ECC. To reduce the latency, the comparison of the data is parallelized with the encoding process that generates the parity information. The parallel operations are enabled based on the fact that the systematic codeword has separate fields for the data and parity. In addition, an efficient processing architecture has been presented to further minimize the latency and complexity.
Therefore a reasonable reduction in power is achieved with the proposed design.

REFERENCES

Designing of Fast Multiplication System for RNS (Cryptography)

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Abstract—Communication security is very important in day to day life. The proposed algorithms and architectures operate on Galois Fields GF of the form GF(p) for integers and GF(2^n) for polynomials. Alternative number representation systems such as Residue Number System for integers and Polynomial Residue Number System for polynomials are employed, as well as a VLSI architecture of a dual-field residue arithmetic Montgomery multiplier are presented. An analysis of input/output conversions to/from residue representation, along with the proposed residue Montgomery multiplication algorithm, reveals common multiply-accumulate data paths both between the converters and between the two residue representations. A versatile architecture is derived that supports all operations of Montgomery multiplication like input/output conversions, Mixed Radix Conversion for integers and polynomials, in the same hardware. Detailed comparisons with state-of-the-art implementations prove the potential of residue arithmetic exploitation in dual-field modular multiplication.

I. INTRODUCTION

The computation of the Montgomery exponentiation (ME) in the Residue Number System (RNS) sanctions constraining the delay due to carry propagation and reaching a high degree of parallelism. This approach mainly requires the execution of a set of Montgomery multiplications (MMs). However, in RNS, some operations (e.g. division, comparison, modulo) are natively arduous to execute. Hence, several approaches have been proposed in order to plenarily exploit the potential of RNS for modular exponentiation, by minimizing the impact of cognate drawbacks. A key element of these approaches is the Base Extension (BE), which calculates a number on a different RNS base.

A paramount number of applications including cryptography, error rectification coding, computer algebra, DSP, etc., rely on the efficient realization of arithmetic over finite fields of the form GF(2^n), where n ∈ Z and n ≥ 1, or the GF(p) form, where p a prime. Cryptographic applications form a special case, since, for security reasons, they require immensely colossal integer operands efficient field multiplication with astronomically immense operands is crucial for achieving a satiating cryptosystem performance, since multiplication is the most time- and area-consuming operation. Therefore, there is a desideratum for incrementing the speed of cryptosystems employing modular arithmetic with the least possible area penalty. A flamboyantly discernible approach to achieve this would be through parallelization of their operations. In recent years, RNS and PRNS have relished renewed scientific interest due to their ability to perform expeditious and
parallel modular arithmetic. Utilizing RNS/PRNS, a given path accommodating an astronomically immense data range is superseded by parallel paths of more diminutive dynamic ranges, with no desideratum for exchanging information between paths. As a result, the utilization of residue systems can offer reduced involution and power consumption of arithmetic units with sesquipedal word lengths. On the other hand, RNS/PRNS implementations bear the extra cost of input converters to translate numbers from a standard binary format into residues and output converters to translate from RNS/PRNS to binary representations.

An incipient methodology for embedding residue arithmetic in a dual-field Montgomery modular multiplication algorithm for integers in GF(p) and for polynomials in GF(2^n) is presented in this paper. The mathematical conditions that need to be satiated for a valid RNS/PRNS incorporation are examined. The derived architecture is highly parallelizable and multifarious, as it fortifies binary-to-RNS/PRNS and RNS/PRNS-to-binary conversions, Commixed Radix Conversion (MRC) for integers and polynomials, dual-field Montgomery multiplication, and dual-field modular exponentiation and inversion in the same hardware.

II. Cryptography Work

A cryptographic algorithm, or cipher, is a mathematical function utilized in the encryption and decryption process. A cryptographic algorithm works in cumulating with a key—a word, number, or phrase—to encrypt the plaintext. The same plaintext encrypts to different cipher text with different keys.

The security of encrypted data is entirely dependent on two things: the vigor of the cryptographic algorithm and the secrecy of the key.

A cryptographic algorithm, plus all possible keys and all the protocols that make it work comprise a cryptosystem. PGP is a cryptosystem. Cryptosystem can be divided into Software and Hardware.

RESIDUE NUMBER SYSTEM

A cryptographic algorithm, or cipher, is a mathematical function utilized in the encryption and decryption process. A cryptographic algorithm works in cumulating with a key—a word, number, or phrase—to encrypt the plaintext. The same plaintext encrypts to different cipher text with different keys.

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CRYTOSYSTEM

SOFTWARE            HARDWARE

Figure 1. Using symmetric algorithms, the sender and receiver use the same key for encryption and decryption functions.

Residue Number System is an unconventional system. In this system, an integer X is represented by its reminder modulo a number of different bases. These residue numbers are smaller than the original number in the conventional system, so computations can be done with more speed and low power. The advantages of RNS for implementing digital signal processors for certain applications such as FIR filtering are well-known]. Some of the more recent applications have been for 1-D filtering, 2-D filtering, video filtering [10], RSA cryptography, Elliptic curve cryptography, m-ary orthogonal keyed
communication scheme general purpose RISC DSP and Image processing. The RNS is determined using a set of relative pair wise prime integers positive co-prime integers \{m_1, m_2, ..., m_n\} as moduli set. The dynamic range \(M\) of that system is given as a product of the moduli \(m_i\) where \(1 = \prod_{i=1}^{n} m_i M = 1\). Any integer \(X\) between 0 and \(M\) represented as \(x_1, x_2, ..., x_n\). The residues \(x_i\) also called residue digits, are defined as \(x_i mod m_i\).

III. Montgomery Multiplication

In modular arithmetic computation, Montgomery modular multiplication, more commonly referred to as Montgomery multiplication, is a method for performing fast modular multiplication, introduced in 1985 by the American mathematician Peter L. Montgomery. Given two numbers \(a\) and \(b\) modulo a positive integer \(N\), Montgomery multiplication computes \(ab mod N\).

Montgomery multiplication requires converting \(a\) and \(b\) into a special representation called Montgomery form. Because of the overhead involved in the conversion, computing a single product by Montgomery multiplication is slower than computing the product in the integers and performing a modular reduction by division or Barrett reduction. However, when many products are required, as in modular exponentiation, the conversion to Montgomery form becomes a negligible fraction of the time of the computation, and performing the computation by Montgomery multiplication is faster than the available alternatives. Many important cryptosystems such as RSA and Diffie–Hellman key exchange are based on arithmetic operations modulo a large number, and for these cryptosystems, the increased speed afforded by Montgomery multiplication can be important in practice.

Let \(N\) denote a positive integer modulus. The ring \(\mathbb{Z}/N\mathbb{Z}\) consists of residue classes modulo \(N\), that is, sets of the form:
\[
\{a + kN : k \in \mathbb{Z}\}
\]
where \(a\) is some fixed integer. Each residue class is a set of integers such that the difference of any two integers in the set is divisible by \(N\) (and the residue class is maximal with respect to that property; integers aren’t left out of the residue class unless they would violate the divisibility condition). The residue class corresponding to \(a\) is denoted \(\overline{a}\). Equality of residue classes is called congruence and is denoted:
\[
\overline{a} \equiv \overline{b} \pmod{N}.
\]

Storing an entire residue class on a computer is impossible because the residue class has infinitely many elements. Instead, residue classes are stored as representatives. Conventionally, these representatives are the integers \(a\) for which \(0 \leq a \leq N - 1\). If \(a\) is an integer, then the representative of \(\overline{a}\) is written \(a \pmod{N}\). When writing congruences, it’s common to identify an integer with the residue class it represents. With this convention, the above equality is written:
\[
a \equiv b \pmod{N}.
\]

IV. Proposed Design Of Dmas And Dm

A Dual-field Full Adder (DFA) cell is basically a Full Adder (FA) cell consists
of half adder and equipped with a field select signal \( f_{sel} \), that controls the operation mod. When \( f_{sel} = 0 \), the carry output is forced to 0 and the sum outputs the XOR operation of the inputs. As already mentioned, this is equivalent to the addition operation in GF(2\(n\)). When \( f_{sel} = 1 \), GF(p) mode is selected and the cell operates as a normal FA cell.

![Fig. 4.1. Dual-field full-adder cell (DFA).](image)

Dual-field adders in various configurations (carry-propagate, carry-skip, etc) can be mechanized by utilizing DFA cells. In the proposed implementation, 3-level, CLA with 4-bit Carry Look ahead Generator (CLG) groups are employed. An example of a 4-bit dual-field CLA is shown below. The GAP modules generate the signals \( p_i = x_i \text{ XOR } y_i \), \( g_i = x_i \text{ AND } y_i \), \( a_i = x_i \text{ OR } y_i \), and AND gates along with a \( f_{sel} \) signal control whether to eliminate carries or not. The carrylook ahead generator is an AND -OR network.

The MRC-based algorithm avoids the evaluation of the \( \square \) factor of the basis of the proposed RNS-based Montgomery multiplication algorithm. The derived algorithm is identical to Algorithm; however the BC algorithm is now based on the modified version of MRC. Comparing the previous approach employing, which requires L \((L-1)/2\) modular multiplications, the optimized MRC requires only L-2 modular multiplications. The methodology is further extended for the case of GF (2\(n\)).

![Fig. 4.2. Dual-field CLA.](image)

A parallel tree multiplier, which is suitable for high-speed arithmetic, and requires little modification to support both fields, is considered in the proposed architecture. Regarding input operands, either integers or polynomials, partial product generation is common for both fields, i.e., an operation among all operand bits. Consequently, the addition tree that sums the partial products must support both formats. In GF(2\(n\)) mode, if DFA cells are used, all carries are eliminated and only xor operations are performed among partial products. In GF(p) mode, the multiplier acts as a conventional tree multiplier. A 4 X 4-bit example of the proposed dual-field multiplier (DM) with output in carry-save format is depicted in Fig. 4.3.
V. Experimental Results

A dual-field full-adder (DFA) cell is basically a full-adder (FA) cell consists of half adder and the behavior is similar to normal full adder. The Dual field full adder wave form is shown below. The operation is mainly depends on fsel. The dual field of G(2n) and G(p) can be performed easily in this method.

Fig. 4.3. Dual-field modular/normal adder/subtractor (DMAS).

Fig. 4.4. Dual-field multiplier (DM).

Fig. 5.1 Dual Field Full Adder
An example of a 4-bit dual-field CLA is shown below. The GAP modules generate the signals \( p_i = x_i \text{ XOR } y_i \), \( g_i = x_i \text{ AND } y_i \), \( a_i = x_i \text{ OR } y_i \), and AND gates along with a fsel signal control whether to eliminate carries or not. The carry-look ahead generator is an AND -OR network. This CLA is useful to design the DMAS whose waveform is shown below.

Fig. 5.2 CLA waveform
The work presented in this paper the Dual-field Full Adder consists of When \( \text{fsel} = 0 \), the carry output is forced to 0 and the sum outputs the XOR operation of the inputs. When \( \text{fsel} = 1 \), GF(p) mode is selected and
the cell operates as a normal FA cell. The duel full adder result is shown below.

Fig. 5.3 Simulation result of DMAS

The work presented in this paper, the DM multiplier which is suitable for high-speed arithmetic requires little modification to support both fields. A 4 4-bit example of the proposed dual-field multiplier (DM) with output in carry-save format is depicted.

Fig. 5.4 Result of DM

V. CONCLUSIONS

The design methodology for incorporating RNS and PRNS in MMM in GF(p) or GF(2n) respectively was subsequently presented. An analysis of input/output conversions to/from residue representation, along with the proposed residue Montgomery multiplication algorithm, revealed common multiply-accumulate data paths both between the converters and between the two residue representations. A novel versatile architecture was derived that supports all operations of MM in GF(p) and GF(2n), input/output conversions, MRC for integers and polynomials, dual-field modular exponentiation and inversion in the same hardware. Detailed comparisons with state-of-the-art implementations proved the potential of residue arithmetic exploitation in dual-field modular multiplication.

REFERENCES


Designing of Multi Band Clock Distribution for SOC/NOC Application

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Abstract: The clock distribution network consumes nearly 70% of the total power consumed by the integrated circuit since this is the only signal which has the highest switching activity. Normally for a multiband clock domain network we develop a multiple PLL, this project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is modeled using Verilog simulated using Modelsim and implemented and synthesized using Xilinx tool.

1. INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands, such as HIPER LAN II and Network standards like a 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like Network protocol 802.15.4 are recognized for low-rate data transmissions. The integrated synthesizers for Wireless LAN applications at 5 GHz reported in and consume up to 24 mw in CMOS realizations, where the first-stage divider is implemented using an Injection-locked divider which consumes large chip area and has a narrow locking range. The best published frequency synthesizer at 5 GHz consumes 9.6 mw at 1-V supply, where its complete divider consumes power around 6 mw, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating Frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers.

High speed divide-by-counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide-by-counter consists of flip-flops (FF) and extra logic, which determines the terminal count. Conventional high speed FF based divide by counter designs use current-mode logic (CML) latches and suffer from the disadvantage of large load capacitance. This not only limits the maximum operating frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true-single-phase clock (TSPC). The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra P-MOS/N-MOS transistor can form an integrated function of FF and AND/OR logic. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design. These two classic designs each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a rationed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in adopt a general TSPC logic family containing both rationed and ratio less inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario. In a power gating technique by inserting an
extra PMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations. Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. In particular, here focus on low operations for power saving without sacrificing the speed performance. In this design, rationed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic. The proposed design in capable of working at a maximum frequency of 531 MHz when the supply voltage is as low as 0.6 V.

2. DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

$$f_{\text{max}} = \frac{1}{t_{\text{pLH}} + t_{\text{pHL}}}$$

Where $t_{\text{pLH}}$ and $t_{\text{pHL}}$ are the propagation delays of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{\text{switching}} = \sum_{i=1}^{n} f_{\text{clk}} C_{L_i} V_{dd}^2$$

where $n$ is the number of switching nodes, $f_{\text{clk}}$ is the clock frequency, $C_{L_i}$ is the load capacitance at the output node of the stage, and $V_{dd}$ is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{\text{sc}} = I_{\text{sc}} * V_{dd}$$

where $I_{\text{sc}}$ is the short-circuit current. The analysis in shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-μm CMOS process.

3. WIDEBAND E-TSPC 2/3 PRESCALER

The E-TSPC 2/3 prescaler consumes large short circuit power and has a higher frequency of operation

Proposed dynamic logic multiband flexible divider.

The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz. The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25 mw. Most Network protocol 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage, while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multi modulus 32/33/47/48 prescaler as shown in Fig. 1. The divider also uses an improved low power loadable bit-cell for the Swallow-counter.
than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design do not consist of two D-flip-flops and two NOR gates embedded in the flip flops. The first NOR gate is embedded in the last on DFF1, and the second NOR gate is embedded in the first stage of DFF2.

1. Wideband single-phase clock 2/3 prescaler.

The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2. The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

\[ C_{L\text{-wideband}} = C_{L2} + C_{L3} + 2C_dM2 + C_dM1 + 2C_g1 \]

When MC switches from "0" to "I," transistors M2,M4 and Ms in DFF1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

\[ P_{\text{wideband divide-by-2}} = \sum f_{out} C_{L2} Vdd^2 P_{SC1} + P_{SC2} \]

Where \( C_{L2} \) is the load capacitance at the output node of the ith stage of DFF2, and PSC1 and PSC2 are the short-circuit power in the second and third stages of DFF2. When logic signal MC switches from "I" to "0." the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

4. MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.
Proposed Multimodulus 32/33/47/48 Prescaler

The multimodulus prescaler consists of the wideband 2/3 \((N/(N+1))\) prescaler, four asynchronous TSPC divide-by-2 circuits \((AD=16)\) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling \(N/(N+1)\) divisions, the additional control signal \(sel\) is used to switch the prescaler between 32/33 and 47/48 modes.

1) Case 1: \(sel='0'\)

When \(sel='0'\), the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If \(MC=1\), the 2/3 prescaler operates in the divide-by-2 mode and when \(MC=0\), the 2/3 prescaler operates in the divide-by-3 mode. If \(MOD=1\), the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for the entire operation. The division ratio \(N\) performed by the multimodulus prescaler is

\[
N = (AD*N1)+(0*(N1+1)) = 32
\]

Where \(N1=2\) and \(AD=16\) is fixed for the entire design. If \(MOD=0\), for 30 input clock cycles \(MC\) remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, \(MC\) remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio \(N+1\) performed by the multi modulus prescaler is and

\[
N+1 = ((AD-1)*N1)+(1*(N1+1)) = 33
\]

2) Case 2: \(sel='1'\)

When \(sel='1'\), the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If \(MC=1\), the 2/3 prescaler operates in divide-by-3 mode and when \(MC=0\), the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when \(sel='0'\). If \(MOD=1\), the division ratio \(N+1\) performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

\[
N+1 = (AD*(N1+1))+(0*N1) = 48
\]

If \(MOD=0\), the division ratio \(N\) performed by the multimodulus prescaler is

\[
N = ((AD-1)*(N1+1))+(1 * N1) = 47
\]

MULTITBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Fig 1 consists of the multi modulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz).

A. SWALLOW (S) COUNTER:

The 6-bit s-counter shown in Fig 4 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design. It is similar to the bit-cell except it uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S1...
divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles. During a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation. this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S counter for a period of \((N\times(P-S))\) clock cycles. Here, the programmable input (PI) is used to load the counter.

B. PROGRAMMABLE (P) COUNTER :

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band (5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

### Results and Conclusion

**Table I**

<table>
<thead>
<tr>
<th>Sel</th>
<th>MOD</th>
<th>MC</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Divide-by-2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Divide-by-3</td>
</tr>
</tbody>
</table>

1) When Sel=0:

When Sel=0 the output from N4 gate is given to the

---

**Programmable (P) Counter**
prescaler and the multimodal’s prescaler selects 32/33 mode and the division ratio is controlled by MOD signal. When MOD=1 the output from N4 gate switches to logic ‘1’ and the prescaler operates in divide-by-2 for entire operation. i.e., now division ratio of 32 (N) is performed. Similarly when MOD=0, MC remains high for first 30 input clock cycles and goes low for 3 input clock cycles. Thus division ratio of 33(N+1) is performed. N and N+1 are given by

\[ N = (AD \times N1) = 32 \]
\[ N + 1 = ((AD -1) \times N1) + (1 \times (N1 + 1)) = 33 \]

2) When Sel=1:

When Sel=1, the inverted output from N4 gate is given to the input of 2/3 prescaler and multimodal’s prescaler operates in 47/48 mode. MOD signal controls the division ratio. When MOD=1 and MC=1 prescaler operated in divide-by-3 for the entire input cycles and division ratio of 48 (N+1) is performed. When MOD=1 and MC=0 divideby-2 is selected for entire input clock cycles for prescaler and the division ratio of 47(N) is performed. N and N+1 are given by

\[ N = ((AD -1) \times (N1 + 1)) + (1 \times 2 \times N1) = 47 \]
\[ N + 1 \times (AD \cdot (N1 + 1)) = 48 \]

6. SIMULATED RESULT

6. CONCLUSION

In this paper a simple approach for the low power single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies. Here the clock divider uses a wide band 2/3 prescaler and a multimodal’s prescaler. By using this multimodal’s prescaler.
REFERENCE

Designing of Self Timed Adder by Using CMOS Technology

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Abstract: In today’s world there is a great need for low power design and area efficient high performance in DIP (Digital Image Processing) system. In this paper the proposed method presents a parallel single-rail self-timed adder. It uses recursive method for performing multi bit binary addition. This design attains good performance without any special speedup circuitry. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fan outs. The recursive method based adder consumes least power among other Self-timed adders. In our work this can be reduced with proposed adder. This technique presents a pre-processing and post processing adder to minimize the multiplier technique. A high fan-in gate is required though but this is unavoidable for asynchronous logic and is managed by connecting the transistors in parallel. Simulations have been performed using cadence tool and superiority of the proposed approach over existing asynchronous adders. In this proposed system we are using a parallel prefix adder it is used to reduce the power consumption, area efficiently. Simulation of this technique is carried out by the Dsch and micro wind

I. INTRODUCTION

Binary addition is the single most important operation that a processor performs. Most of the adders have been designed for synchronous circuits even though there is a strong interest in clockless/ asynchronous processors/circuits [1]. Asynchronous circuits do not assume any quantization of time. Therefore, they hold great potential for logic design as they are free from several problems of clocked (synchronous) circuits. In principle, logic flow in asynchronous circuits is controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks. Explicit handshaking blocks for small elements, such as bit adders, are expensive. Therefore, it is implicitly and efficiently managed using dual-rail carry propagation in adders. A valid dual-rail carry output also provides acknowledgment from a single-bit adder block. Thus, asynchronous adders are either based on full dual-rail encoding of all signals (more formally using null convention logic [2] that uses symbolically correct logic instead of Boolean logic) or pipelined operation using single-rail data encoding and dual-rail carry representation for acknowledgments. While these constructs add robustness to circuit designs, they also introduce significant overhead to the average case performance benefits of asynchronous adders. Therefore, a more efficient alternative approach is worthy of consideration that can address these problems. This brief presents an asynchronous parallel self-timed adder (PASTA) using the algorithm originally proposed in [3]. The design of PASTA is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is suitable for VLSI implementation. The design works in
a parallel manner for independent carry chain blocks. The implementation in this brief is unique as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder. Cyclic circuits can be more resource efficient than their acyclic counterpart. On the other hand, wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs before the outputs are stabilized. The proposed circuit manages automatic single-rail pipelining of the carry inputs separated by propagation and inertial delays of the gates in the circuit path. Thus, it is effectively a single rail wave-pipelined approach and quite different from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals.

II. Self-timed adder:

There are a myriad designs of binary adders and we focus here on asynchronous self-timed adders. Self-timed refers to logic circuits that depend on and/or engineer timing assumptions for the correct operation. Self-timed adders have the potential to run faster averaged for dynamic data, as early completion sensing can avoid the need for the worst case bundled delay mechanism of synchronous circuits. They can be further classified as follows. A. Pipelined Adders Using Single-Rail Data Encoding The asynchronous Req/Ack handshake can be used to enable the adder block as well as to establish the flow of carry signals. In most of the cases, a dual-rail carry convention is used for internal bitwise flow of carry outputs. These dual-rail signals can represent more than two logic values (invalid, 0, 1), and therefore can be used to generate bit-level acknowledgment when a bit operation is completed. Final completion is sensed when all bit Ack signals are received (high). The carry-completion sensing adder is an example of a pipelined adder [8], which uses full adder (FA) functional blocks adapted for dual-rail carry. On the other hand, a speculative completion adder is proposed in [9]. It uses so-called abort logic and early completion to select the proper completion response from a number of fixed delay lines. However, the abort logic implementation is expensive due to high fan-in requirements. B. Delay Insensitive Adders Using Dual-Rail Encoding Delay insensitive (DI) adders are asynchronous adders that assert bundling constraints or DI operations. Therefore, they can correctly operate in presence of bounded but unknown gate and wire delays [2]. There are many variants of DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are assumed to increase complexity. Though dual-rail encoding doubles the wire complexity, they can still be used to produce circuits nearly as efficient as that of the single-rail variants using dynamic logic or NMOS only designs. An example 40 transistors per bit DIRCA adder is presented in [8] while the conventional CMOS RCA uses 28 transistors. Similar to CLA, the DICLA defines carry propagate, generate, and kill equations in terms of dual-rail encoding [8]. They do not connect the carry signals in a chain but rather organize them in a hierarchical tree. Thus, they can potentially operate faster when there is long carry. A further optimization is provided from the observation that dualrail encoding logic can benefit from settling of either the 0 or 1 path. Dual-rail logic need not wait for both
paths to be evaluated. Thus, it is possible to further speed up the carry look-ahead circuitry to send carry-generate/carry-kill signals to any level in the tree. This is elaborated in [8] and referred as DICLA with speedup circuitry (DICLASP).

III. PASTA
the architecture and theory behind PASTA is presented. The adder first accepts two input operands to perform half additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

Fig. 1. General block diagram of PASTA
The general architecture of the adder is shown in Fig. 1. The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values.

IV. Recursive Formula for Binary Addition
Let $S_i^j$ and $C_{i+1}^j$ denote the sum and carry, respectively, for $i$th bit at the $j$th iteration. The initial condition ($j = 0$) for addition is formulated as follows:

$$S^0 = a_i \text{ xor } b_i$$

$$C_{i+1}^0 = a_i b_i \text{. (1)}$$

The $j$th iteration for the recursive addition is formulated by

$$S_i^j = S_i^{j-1} \text{ xor } C_i^{j-1}, \text{ } 0 \leq i < n \text{ (2)}$$

$$C_{i+1}^j = S_i^{j-1} C_i^{j-1}, \text{ } 0 \leq i \leq n \text{. (3)}$$

The recursion is terminated at $k$th iteration when the following condition is met:

$$C_n^k + C_{n-1}^k + \ldots + C_1^k = 0, \text{ } 0 \leq k \leq n \text{. (4)}$$

Now, the correctness of the recursive formulation is inductively proved as follows.

Theorem 1: The recursive formulation of (1)–(4) will produce correct sum for any number of bits and will terminate within a finite time.

Proof: We prove the correctness of the algorithm by induction on the required number of iterations for completing the addition (meeting the terminating condition).

Basis: Consider the operand choices for which no carry propagation is required, i.e., $C_i^j = 0$ for all $i \in [0..n]$. The proposed formulation will produce the correct result by a single-bit computation time and terminate instantly as (4) is met.

Induction: Assume that $C_{i+1}^k = 0$ for some $i$th bit at $k$th iteration.
Let \( l \) be such a bit for which \( C_{k+l}^l = 1 \). We show that it will be successfully transmitted to next higher bit in the \((k+1)\)th iteration. As shown in the state diagram, the \( k \)th iteration of \( l \)th bit state \((C_{k+l}^l, S_{k+l}^l)\) and \((l+1)\)th bit state \((C_{k+l+2}^l, S_{k+l+1}^l)\) could be in any of \((0, 0)\), \((0, 1)\), or \((1, 0)\) states.

As \( C_{k+1}^l = 1 \), it implies that \( S_{k+1}^l = 0 \). Hence, from (3), \( C_{k+1+l+1}^l = 0 \) for any input condition between 0 to \( l \) bits.

We now consider the \((l+1)\)th bit state \((C_{k+l+2}^l, S_{k+l+1}^l)\) for \( k \)th iteration. It could also be in any of \((0, 0)\), \((0, 1)\), or \((1, 0)\) states. In \((k+1)\)th iteration, the \((0, 0)\) and \((1, 0)\) states from the \( k \)th iteration will correctly produce output of \((0, 1)\) following (2) and (3). For \((0, 1)\) state, the carry successfully propagates through this bit level following (3). Thus, all the single-bit adders will successfully kill or propagate the carries until all carries are zero fulfilling the terminating condition. The mathematical form presented above is valid under the condition that the iterations progress synchronously for all bit levels and the required input and outputs for a specific iteration will also be in synchrony with the progress of one iteration. In the next section, we present an implementation of the proposed architecture which is subsequently verified using simulations.

A CMOS implementation for the recursive circuit is shown in Fig. 3. For multiplexers and AND gates we have used TSMC library implementations while for the XOR gate we have used the faster ten transistor implementation based on transmission gate XOR to match the delay with AND gates, then we have to implement ha adder bye 10 transistor ,and mux design by 12 tansisitors. Here we implementing recursive self timed adder with half adder and mux design. Then we can avoid delay. Normal adder design. Below showing those designs.

Fig 2: half adder module

Fig3 : mux module

V. Simulation result
manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. Simulation results are used to verify the advantages of the proposed approach.

REFERENCES


GSM Based Automatic Energy Meter Reading System with Instant Billing

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Abstract: The Household data automatically reading is significant in the process of power system information. It is also an urgent problem that power industries want to solve because the accuracy and real time of meter data copy affect the power system information level, management decisions, and economic benefits. Recently there have been many reports concerning the automatic meter reading. Nowadays the energy meter monitoring and taking of the readings need lots of manual power. To reduce the manual power we are going for the proposed system.

In the proposed system we are using the ARM microcontroller for the efficient energy meter monitoring system. This system is connected with the energy meter with load. The IR receiver is used to count the reading of the energy meter. The value of the IR receiver will be given to the microcontroller. If the user wants to recharge the system he has to send the command to the GSM modem. If the amount is too low then the system will send the alert message to the user mobile number via GSM modem. The status will be displayed in LCD which is interfaced with the microcontroller. Meanwhile if any low voltage occurs in the supply the supply is switched off using relay circuit.

I.INTRODUCTION

The Household data automatically reading is significant in the process of power system information. It is also an urgent problem that power industries want to solve because the accuracy and real time of meter data copy affect the power system information level, management decisions, and economic benefits. Recently there have been many reports concerning the automatic meter reading. Nowadays the energy meter monitoring and taking of the readings need lots of manual power. To reduce the manual power we are going for the proposed system.

Now-a-days technology has developed to a large extend. At the same time the need for systems with automation and high security are preferred. So, by using one of the best technologies available i.e. GSM we are designing an automatic power meter reading system for commercial and domestic purposes. For paying electricity bills we have to go to e-seva for paying the bills, this is very time consuming process and in electrical department side there may be a chance of errors in noting the units and issue of monthly bills. By using this project we can avoid such problems.

The development of a GSM Automatic Power Meter Reading (GAPMR) system is presented in this paper. The GAPMR system is consists of GSM digital Power meters installed in every consumer unit and an electricity ebilling system at the energy provider side. The GSM Digital Power Meter (GPM) is a single phase digital kWh power meter with embedded GSM Modem which utilizes the GSM network to send its
power usage reading using Short Messaging System (SMS) back to the energy provider wirelessly. A working prototype of the GAPMR system was build to demonstrate the effectiveness and efficiency of automatic meter reading, billing and notification through the use of GSM network.

This project is aimed to develop a system to provide security by intimating the condition in the form of SMS by making use of GSM technology. This project makes use of a GSM transceiver to send the messages resembling the condition. According to this system, the mobile no. of concerned person will be stored in the microcontroller.

The main objective of this project is to design a prepaid energy meter system with the help of GSM technology. For measuring energy consumed by the user we are going to use one digital energy meter, at the same time as it uses 1 unit the count will be displayed in LCD. Up to end of month no of units consumed and total amount to be pay will update according to the power consumption and at the end of the month total amount will transferred to last month due Coloum. And if the customer not paid that money within the 15 days then we will trip the total power supply connected to load and we will give intimation to the customer through GSM SMS. We will provide the supply to customer when only he pays the bill.

II. GSM Technology:

2.1 Definition of GSM:

GSM (Global System for Mobile communication) is an open, digital cellular technology used for transmitting mobile voice and data services.

GSM (Global System for Mobile communication) is a digital mobile telephone system that is widely used in Europe and other parts of the world. GSM uses a variation of Time Division Multiple Access (TDMA) and is the most widely used of the three digital wireless telephone technologies (TDMA, GSM, and CDMA). GSM digitizes and compresses data, then sends it down a channel with two other streams of user data, each in its own time slot. It operates at either the 900 MHz or 1,800 MHz frequency band. It supports voice calls and data transfer speeds of up to 9.6 kbit/s, together with the transmission of SMS (Short Message Service).

2.2 GSM Modem:

A GSM modem is a wireless modem that works with a GSM wireless network. A wireless modem behaves like a dial-up modem. The main difference between them is that a dial-up modem sends and receives data through a fixed telephone line while a wireless modem sends and receives data through radio waves.

Fig 2.1 gsm modem

A GSM modem can be an external device or a PC Card / PCMCIA Card. Typically, an external GSM modem is connected to a computer through a serial cable or a USB cable. A GSM modem in the form of a PC Card / PCMCIA Card is designed for use with a laptop computer. It should be inserted into one of the PC Card / PCMCIA Card
slots of a laptop computer. Like a GSM mobile phone, a GSM modem requires a SIM card from a wireless carrier in order to operate.

**III. Project description**

3.1 ARM7 (LPC2148): The LPC2141/2/4/6/8 microcontrollers are based on a 32/16 bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combines the microcontroller with embedded high speed flash memory ranging from 32 Kb to 512 Kb. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30% with minimal performance penalty.

Due to their tiny size and low power consumption, LPC2141/2/4/6/8 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. A blend of serial communications interfaces ranging from a USB 2.0 Full Speed device, multiple UARTs, SPI, SSP to I2Cs, and on-chip SRAM of 8 KB up to 40 KB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems.

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**3.2 Circuit Diagram & Implementation**

![LPC2148 Interface](image1)

Fig:3.2.1 LPC2148 Interface

![GSM Interface](image2)

Fig:3.2.2 GSM Interface
The Household data automatically reading is significant in the process of power system information. It is also an urgent problem that power industries want to solve because the accuracy and real time of meter data copy affect the power system information level, management decisions, and economic benefits. Recently there have been many reports concerning the automatic meter reading. Now days the energy meter monitoring and taking of the readings need the lots of manual power. To reduce the manual power we are going for the proposed system.

3.3 BLOCK DIAGRAM

Home section:

EB Section:
In the proposed system we are using the ARM microcontroller for the efficient energy meter monitoring system. This system is connected with the energy meter with load. The IR receiver is used to count the reading of the energy meter. The value of the IR receiver will be given to the microcontroller. If the user wants to recharge the system he has to send the command to the GSM modem. If the amount is too low then the system will send the alert message to the user mobile number via GSM modem. The status will be displayed in LCD which is interfaced with the microcontroller. Meanwhile if any low voltage occurs in the supply the supply is switched off using relay circuit.

CONCLUSION

The implementation of Gsm based automatic energy meter reading system with instant billing is done successfully. The communication is properly done without any interference between different modules in the design. Design is done to meet all the specifications and requirements. Software tools like Keil Uvision Simulator, Proload to dump the source code into the microcontroller, Orcad Lite for the schematic diagram have been used to develop the software code before realizing the hardware.

Various electronic meters have been developed and are still being developed. However the use of GSM in this particular system provides numerous advantages over methods that have been previously used. Data transmission is charged at standard SMS rates, thus the charges are not based on the duration of data transmission. The cost efficient transmission of readings ensures that power consumption values can be transmitted more frequently to a remote station. The implications of being able to transmit readings more often are that energy utilities will be able to generate timely bills, better understand energy demand patterns, manage meter failures more efficiently and manage fraud better.

It can be concluded that the design implemented in the present work provide portability, flexibility and the data transmission is also done with low power consumption.

FUTURE SCOPE

This will help the to recharge the meter from anywhere by sending just a simple message or through internet. It will more efficient and fast system. This will help theft detection and connect the keypad to change the mobile number.

REFERENCES

Designing of Integer DCT Architectures for HEVC

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ABSTRACT: With this paper, most of us present area- along with power-efficient architectures for your implementation connected with integer under the discrete cosine transform (DCT) connected with unique plans to be used in High Efficiency Video Coding (HEVC). Many of us display make fish an effective regular matrix multiplication structure can often discover parallel architectures intended for 1-D integer DCT connected with unique plans. Many of us furthermore display the suggested construction may be reusable intended for DCT connected with plans some, 8, 16, along with thirty two with a throughput connected with thirty two DCT coefficients for each cycle no matter what the particular transform size. Moreover, the particular suggested architectural mastery may be pruned to reduce the particular difficulty connected with implementation significantly with only a marginal influence about the coding efficiency.

I.INTRODUCTION

The Discrete Cosine Transform (DCT) has been widely applied in the area of image compression and video compression, such as JPEG, MPEG-2/4 and H.263. Its popularity is attributed to its ability to decorrelate data of spatial domain into data of frequency domain. Data will become more compact after being transformed, redundant information can be further removed. The DCT is considered as the closest to K-L transform, which is the ideal energy compaction transform. However, the matrix elements of DCT contain real numbers presented by a finite number of bits, which inevitably leads to the possibility of drift (mismatch between the decoded data in the encoder and decoder). Several methods have been introduced to control the accumulation of drift in video compress standards before H.264. However, H.264 makes extensive use of prediction, which causes it to be very sensitive to drift [2]. In order to eliminate mismatch between encoders and decoders and to facilitate low complexity implementations, latest video standards like H.264, VC-1 and AVS begin to adopt integer transform. High Efficiency Video Coding (HEVC) [3] is the newest standard for high definition video processing. It is considered as the successor of H.264. Main goal of HEVC is to achieve 50% higher coding efficiency than H.264. In order to achieve this goal, HEVC adopts lots of state of the art coding tools including 4/8/16/32 integer transform. Compared to H.264, not only the size of matrices themselves but also matrix elements get larger. This makes the implementation of both hardware and software become very complicated. In this work, a fast algorithm for 8x8 integer transform of HEVC is presented, which is suitable for hardware and software implementation.

Despite the many advantages of digital representation of signals compared
to the analog counterpart, they need a very large number of bits for storage and transmission. For example, a high-quality audio signal requires approximately 1.5 megabits per second for digital representation and storage. A television-quality low-resolution color video of 30 frames per second with each frame containing 640 x 480 pixels (24 bits per color pixel) needs more than 210 megabits per second of storage. As a result, a digitized one-hour color movie would require approximately 95 gigabytes of storage. The storage requirement for upcoming high-definition television (HDTV) of resolution 1280 x 720 at 60 frames per second is far greater. A digitized one-hour color movie of HDTV-quality video will require approximately 560 gigabytes of storage. A digitized 14 x 17 square inch radiograph scanned at 70 pm occupies nearly 45 megabytes of storage. Transmission of these digital signals through limited bandwidth communication channels is even a greater challenge and sometimes impossible in its raw form. Although the cost of storage has decreased drastically over the past decade due to significant advancement in microelectronics and storage technology, the requirement of data storage and data processing applications is growing explosively to outpace this achievement.

2. Compressions

There are two types of compressions

1. Lossless compression

Digitally identical to the original image. Only achieve a modest amount of compression

- Lossless compression involves with compressing data, when decompressed data will be an exact replica of the original data. This is the case when binary data such as executable are compressed.

2. Lossy compression

Discards components of the signal that are known to be redundant. Signal is therefore changed from input

Figure 2.1 Different Types of Lossy Compression Techniques

2.1.1 Discrete Cosine Transform (DCT):

The forward and inverse 2-D DCT can be written as:

\[
Z(u,v) = \frac{2}{N} C(u)C(v) \sum_{i=0}^{N-1} x(i,j) \cos \left( \frac{2 \pi i u}{2N} \right) \cos \left( \frac{2 \pi j v}{2N} \right)
\]  \hspace{1cm} (1)

\[
x(i,j) = \frac{2}{N} \sum_{u=0}^{N-1} \sum_{v=0}^{N-1} Z(u,v) C(u)C(v) \cos \left( \frac{2 \pi i u}{2N} \right) \cos \left( \frac{2 \pi j v}{2N} \right)
\]  \hspace{1cm} (2)

where \(x(ij)\) is the image pixel data, and \(Z(u,v)\) is the transport data.

The 2-D DCT is an orthogonal and separable transform. It can be expressed in matrix notation as two 1-D DCT’s as follows: \(Z = CX(CT)\) and \(X = (CT)ZC\). Therefore, we can decompose (1) into two 1-D DCT’s:
(2) can be decomposed into two 1-D IDCT's:

\[ Z(u, v) = \frac{2}{N} \sum_{x} C(u)Y(v, i) \cos \left( \frac{(2i+1)\pi}{2N} \right) \]  

\[ Y(v, i) = \frac{2}{N} \sum_{y} C(v)Z(u, j) \cos \left( \frac{(2j+1)\pi}{2N} \right). \]

A Standard diagram shown in Figure 2.2 where the computation of the 2-D DCT has been separated into two 1-D DCT's.

Figure 2.2 Standard DCT Computation

3. Algorithm for Hardware Implementation of Integer DCT for HEVC:

In the Joint Collaborative Team Video Coding (JCT-VC), which manages the standardization of HEVC, Core Experiment 10 (CE10) studied the design of core transforms over several meeting cycles. The eventual HEVC transform design involves coefficients of 8-bit size, but does not allow full factorization unlike other competing proposals. It however allows for both matrix multiplication and partial butterfly implementation. In this section, we have used the partial-butterfly algorithm of for the computation of integer DCT along with its efficient algorithmic transformation for hardware implementation.

A. Key Features of Integer DCT for HEVC

The N-point integer DCT 1 for HEVC given by [14] can be computed by a partial butterfly approach using a (N/2)-point DCT and a matrix-vector product of (N/2)×(N/2) matrix with an (N/2)-point vector as

\[
\begin{bmatrix}
s(0) \\
s(1) \\
\vdots \\
s(N-1)
\end{bmatrix} = C_N \begin{bmatrix}
a(0) \\
a(1) \\
\vdots \\
a(N/2-1)
\end{bmatrix}
\]

and

\[
\begin{bmatrix}
y(0) \\
y(1) \\
\vdots \\
y(N-1)
\end{bmatrix} = M_{N/2} \begin{bmatrix}
b(0) \\
b(1) \\
\vdots \\
b(N/2-1)
\end{bmatrix}
\]

where

\[
a(i) = x(i) + x(N - i - 1)
\]

\[
b(i) = x(i) - x(N - i - 1)
\]

for \(i=0,1,\cdots,N/2-1\). \(X=[x(0),x(1),\cdots,x(N-1)]\) is the input vector and \(Y=[y(0),y(1),\cdots,y(N-1)]\) is N-point DCT of \(X\). \(C_{N/2}\) is (N/2)-point integer DCT kernel matrix of size (N/2)×(N/2). \(M_{N/2}\) is also a matrix of size (N/2)×(N/2) and its (i, j)th entry is defined as

\[
m_{N/2}^{i,j} = c_{N}^{2i+1} c_{N}^{-2j} \quad \text{for} \ 0 \leq i, j \leq N/2 - 1
\]

Where \(C_{N}^{2i+1+j}\) is the \((2i+1,j)\)th entry of the matrix \(C_{N}\). Note that (1a) could be similarly decomposed recursively, further using \(C_{N/4}\) and \(M_{N/4}\).

B. Hardware Oriented Algorithm

Direct implementation of (1) requires \(N^2/4 + \text{MUL}_{N/2} + \text{ADD}_{N/2} \) multiplications, \(N^2/4 + N/2 + \text{ADD}_{N/2} \) additions, and 2 shifts where MUL/2 and ADDN/2 are the number of multiplications and additions/subtractions of (N/2)-point DCT, respectively.
Computation of (1) could be treated as a CMM problem [15]-[17]. Since the absolute values of the coefficients in all the rows and columns of matrix Min (1b) are identical, the CMM problem can be implemented as a set of N/2 MCMs that will result in a highly regular architecture and will have low-complexity implementation. The kernel matrices for four-, eight-, 16-, and 32-point integer DCT for HEVC are given in [14], and 4- and eight-point integer DCT are represented, respectively, as

\[
C_4 = \begin{bmatrix}
64 & 64 & 64 & 64 \\
83 & 36 & -36 & -83 \\
64 & -64 & -64 & 64 \\
36 & -83 & 83 & -36 \\
\end{bmatrix}
\]

and

\[
C_8 = \begin{bmatrix}
64 & 64 & 64 & 64 & 64 & 64 & 64 & 64 \\
89 & 75 & 50 & 18 & -18 & -50 & -75 & -89 \\
83 & 36 & -36 & -83 & -83 & -36 & 36 & 83 \\
-18 & -89 & -50 & 89 & 18 & -75 & 75 & -18 \\
64 & -64 & -64 & -64 & 64 & 64 & 64 & 64 \\
50 & -89 & 18 & 75 & -75 & -18 & 89 & -50 \\
36 & -83 & 83 & -36 & -36 & 83 & -83 & 36 \\
18 & -50 & 75 & -89 & 89 & -75 & 50 & -18 \\
\end{bmatrix}
\]

Based on (1) and (2), hardware oriented algorithms for DCT computation can be derived in three stages as in Table I. For 8-, 16-, and 32-point DCT, even indexed coefficients of \([y(0), y(2), y(4), \ldots y(N-2)]\) are computed as 4-, 8-, and 16-point DCTs of \([a(0), a(1), a(2), \ldots a(N/2-1)]\), respectively, according to (1a). In Table II, we have listed the arithmetic complexities of the reference algorithm and the MCM-based algorithm for four-, eight-, 16-, and 32-point DCT. Algorithms for Inverse DCT (IDCT) can also be derived in a similar way.

4. Proposed Architecture for Four-Point Integer DCT:
The proposed architecture for four-point integer DCT is shown in Fig. 4.1(a). It consists of an input adder unit (IAU), a shift-add unit (SAU), and an output adder unit (OAU). The IAU computes \(a(0), a(1), b(0), \) and \(b(1)\) according to STAGE-1 of the algorithm as described in Table I. The computations of \(t_{i,36}\) and \(t_{i,83}\) are performed by two SAUs according to STAGE-2 of the algorithm. The computation of \(t_{0,64}\) and \(t_{1,64}\) does not consume any logic since the shift operations could be rewired in hardware. The structure of SAU is shown in Fig. 4.1(b). Outputs of the SAU are finally added by the OAU according to STAGE-3 of the algorithm.

5. Results:
Fig 5.1: Integer dct wave form

Fig 5.2: Integer dct RTL Schematic

Conclusion:

In this paper, we have proposed area- and power-efficient architectures for the implementation of integer DCT of different lengths to be used in HEVC. The computation of N-point 1-D DCT involves an (N/2)-point 1-D DCT and a vector-matrix multiplication with a constant matrix of size (N/2)×(N/2). We have shown that the MCM-based architecture is highly regular and involves significantly less area-delay complexity and less energy consumption than the direct implementation of matrix multiplication for odd DCT coefficients. We have used the proposed architecture to derive a reusable architecture for DCT that can compute the DCT of lengths 4, 8, 16, and 32 with throughput of 32 output coefficients per cycle.

References

Built-In Generation of Functional Broadside Tests for Multiple Hardware Block on SOC System

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Abstract—When built-in test generation is used for a design that can be partitioned into logic blocks, it is advantageous to identify groups of blocks whose tests have similar characteristics, and use the same built-in test generation logic for the blocks in each group. This paper studies this issue for a built-in test generation method that produces functional broadside tests. Functional broadside tests are important for addressing overtesting of delay faults as well as avoiding excessive power dissipation during test application. The paper discusses the design of the test generation logic for a group of logic blocks, and the selection of the groups.

I. Introduction:

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. While performance and Area remain to be the two major design tolls, power consumption has become a critical concern in today's VLSI system design[1]. The need for low-power VLSI system arises from two major forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices.

Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup.

So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on demand or application some compromise between constraints has to be made. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. In 2002, a new concept of hybrid adders is presented to speed up addition process by Wang et al. that gives hybrid carry look-ahead/carry select adders...
design. In 2008, low power multipliers based on new hybrid full adders is presented.

DESIGN of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

2. Built-In Test Generation

The built-in test generation method brings the circuit into reachable states by initializing the circuit into a state denoted by sinit, which is the initial state of the circuit for functional operation, and applying a primary input sequence A of a fixed length, L, in functional mode.

Test generation procedures for functional and pseudo-functional scan-based tests were described. The procedures generate test sets offline for application from an external tester. Functional scan-based tests use only reachable states as scan-in states. Pseudo-functional scan-based tests use functional constraints to avoid unreachable states that are captured by the constraints. This work considers the on-chip (or built-in) generation of functional broadside tests. On-chip test generation reduces the test data volume and facilitates at-speed test application. On-chip test generation methods for delay faults, such as the ones described, do not impose any constraints on the states used as scan-in states. Experimental results indicate that an arbitrary state used as a scan-in state is unlikely to be a reachable state. The on-chip test generation method from applies pseudo-functional scan-based tests. Such tests are not sufficient for avoiding unreachable states as scan-in states. The on-chip test generation process described in this work guarantees that only reachable states will be used. It should be noted that the delay fault coverage achievable using functional broadside tests is, in general, lower than that achievable using arbitrary broadside tests as in or pseudo-functional broadside tests as in. This is due to the fact that functional broadside tests avoid unreachable scan-in states, which are allowed by the methods described in. However, the tests that are needed for achieving this higher fault coverage are also ones that can cause over testing. They can also dissipate more power than possible during functional operation. Only functional broadside tests are considered in this work. Under the proposed on-chip test generation method, the circuit is used for generating reachable states during test application. This alleviates the need to compute reachable states or functional constraints by an offline process. The underlying observation is related to one of the methods used in for offline test generation.
3 GROUPS OF LOGIC BLOCKS

This section considers the built-in generation of functional broadside tests for groups of logic blocks. The section starts with a discussion of the case where a group $G$ is given. It then considers the selection of groups, and the identification of subsets of seeds for the individual blocks in a group.

(2) The selection of the primary input cube $c_i$ for an individual block $B_i$ is based on a heuristic that attempts to avoid repeated synchronization in $B_i$. It is possible that a different modification of the LFSR sequence, described by a different primary input cube, would yield a higher fault coverage for $B_i$ than the fault coverage based on $c_i$. By accepting that $c_G$ may be different from $c_i$, the procedure for forming the groups explores some of these options. The options it explores have the additional characteristic that they attempt to allow the same cube to be used for several different blocks. Experimental results show that, in some cases, using $c_G$ instead of $c_i$ for a block $B_i$ leads to increased fault coverage for $B_i$ with otherwise the same parameters of the built-in test generation logic. The use of a single primary input cube $c_G$ is complemented by the use of a single set of seeds for all the blocks in the group. This eliminates the need to store distinct sets of seeds for individual blocks. The final design decision that needs to be made is related to the way by which the primary inputs of the blocks in $G$ will be connected to the outputs of the built-in test generation logic. A fixed connection is used in this paper based on the order by which primary inputs appear in the descriptions of the logic blocks. This allows the connection to be determined based on routing considerations. Specifically, for $0 \leq j < n$, output $j$ of the test generation logic drives primary input $j$ of every logic block that has at least $j + 1$ primary inputs. The resulting configuration is illustrated by Fig. 3. In Fig. 3, $B_0$ has $n_0 = 4$ primary inputs, $B_1$ has $n_1 = 2$ primary inputs, $B_2$ has $n_2 = 3$ primary inputs, and $B_3$ has $n_3 = 2$ primary inputs. With $n = 4$, the LFSR has $4d$ bits, and four outputs. The gates corresponding to $c_G$ are not shown in Fig. 3. Output 0 of the test generation logic drives primary input 0 of $B_0$, $B_1$, $B_2$ and $B_3$. Output 1 of the test generation logic drives primary input 1 of $B_0$, $B_1$, $B_2$ and $B_3$. Output 2 of the test generation logic drives primary input 2 of $B_0$ and $B_2$. Output 3 of the test generation logic drives primary input 3 of $B_0$. To compute $c_G | \phi$, 

Fig. 1. Example logic blocks.

Fig. 2. Test generation logic for a group.
for $0 \leq j < n$, the following process is applied. The process assigns the value 0 to primary input $j$ of every logic block that has at least $j + 1$ primary inputs. Using implications, it finds the number of next-state variables that are assigned specified values in all the blocks. Using the same process it finds the number of next-state variables that are assigned specified values when primary input $j$ is assigned the value 1 for every logic block that has at least $j + 1$ primary inputs. The process assigns $c_{G(j)} = 0$ if a 0 results in fewer specified next state variables, $c_{G(j)} = 1$ if a 1 results in fewer specified next-state variables, and $c_{G(j)} = x$ otherwise.

4 Result:

Fig 3. Simulation waveform of LFSR

Fig 4. Simulation waveform of s27

Fig 5. Simulation waveform of top module

Fig 6. RTL schematic of top module

5 Conclusion

The paper studied the built-in generation of functional broadside tests for a design that can be partitioned into logic blocks. In this case, it is advantageous to use the same built-in test generation logic for groups of blocks whose tests have similar characteristics. This implies using the same LFSR, with the same AND and OR gates, and the same seeds, for all the logic blocks in the group. The paper described a procedure for constructing the groups. Considering the set of seeds computed for
a group, the paper also identified subsets of seeds that are required for every logic block individually. This is useful for testing a subgroup, for example, if power considerations require smaller groups of logic blocks to be tested simultaneously, or if some of the logic blocks are disabled due to faults that were detected earlier.

REFERENCES

Designing and Comparative Analyses of Carry Select Adders (CSL, CSL with BEC, CSL with CBL)

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Abstract: In electronics, adder is a digital circuit that performs addition of numbers. To perform fast arithmetic operations, carry select adder (CSA) is one of the fastest adders used in many data-processing processors. The structure of CSA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate-level modification is used in order to reduce the area, delay and power of CSA. The result analysis shows that the proposed structure (csa CBL) is better than the conventional CSA and CSA with BEC.

I. Introduction
Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the binary adder structures have been done, the studies based on their comparative performance analysis are only a few.

II. Carry Select Adder

DESIGN of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry

This is about a digital circuit. For an electronic circuit that handles analog signals see Electronic mixer. In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones’ complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder. Different type of adders as follows
propagated in to the next position . The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin=0 and cin=1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with cin=1 in the regular CSA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2 bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits (MSB’s) two k/2 bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. This technique of dividing adder in to stages increases the area utilization but addition operation fastens.

III. Modified Regular Csa Using BEC

The main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSA. To replace the n bit RCA, an n+1 bit BEC is required. A structure and the function table of a 4 bit BEC are show in Fig and Table II respectively.

![Fig2.1. Regular 16-b SQRT CSA.](image)

**Figure: 4-bit BEC**

<table>
<thead>
<tr>
<th>( B[3:0] )</th>
<th>( X[3:0] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>0001</td>
<td>0001</td>
</tr>
<tr>
<td>( \vdots )</td>
<td>( \vdots )</td>
</tr>
<tr>
<td>1110</td>
<td>1110</td>
</tr>
<tr>
<td>1111</td>
<td>0000</td>
</tr>
</tbody>
</table>

Fig. above illustrates how the basic function of the CSA is obtained by using 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input( (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible
partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & XOR)

\[
\begin{align*}
X_0 &= \sim B_0 \\
X_1 &= \overline{B_0} \cdot B_1 \\
X_2 &= B_2 \oplus (B_0 \cdot B_1) \\
X_3 &= B_3 \oplus (B_0 \cdot B_1 \cdot B_2).
\end{align*}
\]

**Figure 3.1:** modified carry select adder the parallel rca with cin=1 is replaced with bec

**IV. Proposed Csa Using Common Boolean Logic**

To remove the duplicate adder cells in the conventional CSA, an area efficient SQRT CSA is proposed by sharing Common Boolean Logic (CBL) term. While analyzing the truth table of single bit full adder, results show that the output of summation signal as carry-in signal is logic “0” is inverse signal of itself as carry-in signal is logic “1”. It is illustrated by red circles in Table II. To share the Common Boolean Logic term, we only need to implement a XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel.

**TABLE III**

Truth table of single bit full adder, where the upper half part is the case of cin=0 and the lower half part is the case of cin=1

This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified SQRT CSA, the proposed structure is little bit faster. Internal structure of proposed CSA is shown in Fig. 4.1.

**Fig. 4.1** Internal structure of the proposed area-efficient carry select adder is constructed by sharing the common Boolean logic term.
In the proposed SQRT CSA, the transistor count is trade-off with the speed in order to achieve lower power delay product. Thus the proposed SQRT CSA using CBL is better than all the other designed adders. Fig. 9 shows the Block diagram of Proposed SQRT CSA.

\[\text{Fig. 4.2 16-Bit Proposed SQRT CSA using Common Boolean Logic.}\]

\[\text{V. Simulation Result}\]

\[\text{Fig 5.2 Simulation waveforms for existing carry select adder (BEC)}\]

\[\text{Fig 5.3 Simulation waveforms for proposed carry select adder (CBL)}\]

\[\text{CONCLUSION}\]

To perform fast arithmetic operations, carry select adder (CSA) is one of the fastest adders used in many data-processing processors. The structure of CSA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate-level modification is used in order to reduce the area, delay and power of CSA. The result analysis showed that the proposed structure (csa CBL) is better than the conventional CSA and CSA with BEC. All
the ckt are simulated and synthesised by Xilinx ise 14.6.

REFERENCES

Design of Digit-Serial FIR Filters Using Shifting and Adding Method

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Abstract: In the last two decades, many efficient algorithms and architectures have been introduced for the design of low complexity bit-parallel multiple constant multiplications (MCM) operation which dominates the complexity of many digital signal processing systems. On the other hand, little attention has been given to the digit-serial MCM design that offers alternative low complexity MCM operations albeit at the cost of an increased delay. In this paper, we address the problem of optimizing the gate-level area in digit-serial MCM designs and introduce high level synthesis algorithms, design architectures by using Verilog HDL.

I. Introduction

Finite impulse response (FIR) filters are of great importance in digital signal processing (DSP) systems since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high-performance filters. Although both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency. The multiplier block of the digital FIR filter in its transposed where the multiplication of filter coefficients with the filter input is realized, has significant impact on the complexity and performance of the design because a large number of constant multiplications are required. This is generally known as the multiple constant multiplications (MCM) operation and is also a central operation and performance bottleneck in many other DSP systems such as fast Fourier transforms, discrete cosine transforms (DCTs), and error-correcting codes. Although area-, delay-, and power-efficient multiplier architectures, such as Wallace and modified Booth multipliers, have been proposed, the full flexibility of a multiplier is not necessary for the constant multiplications, since filter coefficients are fixed and determined beforehand by the DSP algorithms. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift addition architecture where each constant multiplication is realized using addition/subtraction and shift operations in an MCM operation. For the shift-adds implementation of constant multiplications, a straightforward method, generally known as digit based at the gate level. In this paper, we initially determine the gate-level implementation costs of digit-serial addition, subtraction, and left shift operations used in the shift-adds design of digit-serial MCM operations.
Fig 1: fir filter Transposed form with an MCM block.

II. Shift-adding method

Shift-adding method shift-adds implementation of constant multiplications, a straightforward method, generally known as digit-based recoding [6], initially defines the constants in binary. Then, for each “1” in the binary representation of the constant, according to its bit position, it shifts the variable and adds up the shifted variables to obtain the result. As a simple example, consider the constant multiplications 29x and 43x. Their decompositions in binary are listed as follows:

\[ 29x = (11101)_{\text{bin}} x = 4 + x + 3 + x + 2 + x \]
\[ 43x = (101011)_{\text{bin}} x = 5 + x + 3 + x + 1 + x \]

However, the digit-based recoding technique does not exploit the sharing of common partial products, which allows great reductions in the number of operations and, consequently, in area and power dissipation of the MCM design at the gate level. Hence, the fundamental optimization problem, called the MCM problem, is defined as finding the minimum number of addition and subtraction operations that implement the constant multiplications. Note that, in bit-parallel design of constant multiplications, shifts can be realized using only wires in hardware without representing any area cost.

Experimental results on a comprehensive set of instances show that the solutions of algorithms introduced in this paper lead to significant improvements in area of digit-serial MCM designs compared to those obtained using the algorithms designed for the MCM problem. The digit-serial FIR filter designs obtained by SAFIR also indicate that the realization of the multiplier block of a digit-serial FIR filter under the shift adds architecture significantly reduces the area of digit-serial FIR filters with respect to those designed using digit-serial constant multipliers. Additionally, it is observed that the optimal tradeoff between area and delay in digit-serial FIR filter designs can be explored by changing the digit size d.

III. Design of Digit-Serial MCM Operations Using Digit-Serial Constant Multipliers

Generic digit-serial multiplier architectures in which both operands are time-variant. However, these architectures are not flexible enough to take the advantage of constant multiplications. On the other hand, bit-serial constant multiplier architectures in which one operand is constant (time-invariant). In these constant multiplier architectures, the hardware of the design is significantly reduced with respect to the generic digit-serial multipliers by utilizing the nonzero digits of the constant to be multiplied by the input variable x. Moreover, a CSE technique used to maximize the sharing of partial products among the constant multiplications was also proposed. The digit-serial constant multiplier realized in SAFIR is based on the sequential multiplication algorithm which is illustrated on a simple example in Fig. 2(a). As can be easily seen, this method can be realized by iteratively generating the partial product, i.e., the multiplication of d-bit input data x with the constant c, shifting the partial product, and adding with the previous partial product sum. As depicted in Fig. 2(b), in
our design, at each clock cycle the d-bit input data x (xi) is applied to the select input of the 2d – 1 multiplexer and the partial product is generated at the multiplexer output based on the xi value. Since the constant c is known, rather than using a multiplication operation the inputs of the multiplexer are assigned to the integer values of 0, c, 2c, 3c, ..., (2d – 1)c. Thus, the bitwidth of the multiplexer output, i.e., m, is \( \log_2(2d - 1)c \). The partial product store (PPS) block is a shift register with a total of \( \log_2 c + N \) D flip-flops and its leftmost m bits are assigned to the inputs of the addition operation. When the current partial product (the multiplexer output) is added with the leftmost m bits of the PPS block, the output of the adder is stored in the leftmost D flip-flops of the PPS block and is shifted right by d bits, filling zeros to the leftmost d bits. Note that the carry output bit of the addition operation is always zero due to the d-

Fig. 2. Digit-serial constant multiplier using the sequential multiplication algorithm [17]. (a) Illustrative example. (b) Design architecture.

Left most zero bits at the m-bit output of the PPS block. At the end of \( N/d \) clock cycles, the constant multiplication cx is available at the outputs of D flip-flops in the PPS block. Note that the latency of this architecture is different from that of the shift-adds architecture given in (5). This is because in each clock cycle, except the last one, the d-bits of cx are obtained, and at the last clock cycle the most significant m-bits of cx are generated. In this scheme, we only consider the positive and odd constants. If an even or negative version of a constant is required as an output, it is realized by shifting the related constant or taking its 2’s complement.

IV. Result

Fig 3: Simulation waveform

Fig 4: RTL schematic

Conclusion:
Thus the implementation of digit serial FIR filter was implemented with low complexity MCM architectures for digit sizes \( d = 2, 4 \). Device utilization and delay values are compared for hardware implementation. Hence this MCM approach drastically reduces the system complexity, area and delay and FPGA hardware real time implementation has performed with spartan3 version. Future enhancement of this paper is to design MCM architecture with more coefficient pairs for FIR filter implementation.

References:
Designing of Fast Decimal Multiplication System by Using BCD Codes

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Abstract:-High-performance, area-efficient hardware implementation of decimal multiplication is preferred to slow software simulations in a number of key scientific and financial application areas, where errors caused by converting decimal numbers into their approximate binary representations are not acceptable. Multi-digit parallel decimal multipliers involve two major stages: (i) the partial product generation (PPG) stage, where decimal partial products are determined by selecting the right versions of the pre-computed multiples of the multiplicand, followed by (ii) the partial product accumulation (PPA) stage, where all the partial products are shifted and then added together to obtain the final multiplication product. In this thesis, we propose a parallel architecture for fixed-point decimal multiplications based on the 8421-5421 BCD representation. In essence, we apply a hybrid 8421-5421 recoding scheme to help simplify the computation logic of the PPG. In the following PPA stage, these generated partial products are accumulated using 8421 carry-lookahead adders (CLAs) organized as a tree structure; this organization is a significant departure from the traditional carry-save-adder-based (CSA) approach, which suffers from the problems introduced by extra recoding logic and/or addition circuits needed. In addition to the proposed 8421-5421-based decimal multiplier, we also propose a 4221-based decimal multi-plier that is built upon a novel full adder for 4221 BCD codes; in this design, expensive 4221-to-8421 conversions are no longer needed, and as a result, the operands of this 4221 multiplier can be directly represented in 4221 BCD.

The proposed 16×16 decimal multipliers are compared against other best known decimal multiplier designs in terms of delays and delay-area products with a TSMC 90nm technology. The evaluation results have confirmed that the proposed 8421-5421 multiplier achieves the lowest delay and is the most time-area efficient design among all the existing hardware-based BCD multipliers.

I. INTRODUCTION
Decimal fixed-point and floating-point formats are important in financial, commercial, and user-oriented computing, where conversion and rounding errors that are inherent to floating-point binary representations cannot be tolerated. The new IEEE 754-2008 Standard for Floating-Point Arithmetic, which contains a format and specification for decimal floating-point (DFP) arithmetic, has encouraged a significant amount of research in decimal hardware. Furthermore, current IBM Power and z/System families of microprocessors and the Fujitsu Sparc X microprocessor, oriented to servers and mainframes, already include fully IEEE 754-2008 compliant decimal floating-point units (DFPUs) for
Decimal64 (16 precision digits) and Decimal128 (34 precision digits) formats. Since area and power dissipation are critical design factors in state-of-the-art DFPUs, multiplication and division are performed iteratively by means of digit-by-digit algorithms [4], [5], and therefore they present low performance. Moreover, the aggressive cycle time of these processors puts an additional constraint on the use of parallel techniques for reducing the latency of DFP multiplication in high-performance DFPUs. Thus, efficient algorithms for accelerating DFP multiplication should result in regular VLSI layouts that allow an aggressive pipelining. Hardware implementations normally use BCD instead of binary to manipulate decimal fixed-point operands and integer significands of DFP numbers for easy conversion between machine and user representations. BCD encodes a number X in decimal (non-redundant radix-10) format, with each decimal digit \(X_i \in \{0, \ldots, 9\}\) represented in a 4-bit binary number system. However, BCD is less efficient for encoding integers than binary, since codes 10 to 15 are unused. Moreover, the implementation of BCD arithmetic has more complications than binary, which lead to area and delay penalties in the resulting arithmetic units. A variety of redundant decimal formats and arithmetics have been proposed to improve the performance of BCD multiplication. The BCD carry-save format [9] represents a radix-10 operand using a BCD digit and a carry bit at each decimal position. It is intended for carry-free accumulation of BCD partial products using rows of BCD digit adders arranged in linear or tree-like configurations. Decimal signed-digit (SD) representations, rely on a redundant digit set \(\{\pm 4; \pm 5; \pm 6; \ldots; 0; \ldots; \pm 9\}\), to allow decimal carry-free addition. BCD carry-save and signed-digit radix-10 arithmetics offer improvements in performance with respect to non-redundant BCD. However, the resultant VLSI implementations in current technologies of multioperand adder trees may result in more irregular layouts than binary carry-save adders (CSA) and compressor trees.

Some approaches rely on binary arithmetic to perform decimal multioperand addition and multiplication. In [6], a decimal multioperand adder is implemented using columns of binary compressors and subsequent binary-to-BCD conversions. Also, decimal multioperand addition can be improved using binary carry-save adders and decimal doublers if digits are not represented in BCD but in certain decimal codes, namely, 4221 and 5211. These 4-bit decimal codes satisfy that the sum of the weights of the bits is equal to 9, so that all the 16 4-bit combinations represent a decimal digit in \(\{0, \ldots, 9\}\). These codes have been used to speed-up decimal multioperand addition and multiplication. The additional redundancy available in the 4-bit encoding is used to speed-up BCD operations while retaining the same data path width.

### 2. Redundant BCD Representations

The proposed decimal multiplier uses internally a redundant BCD arithmetic to speed up and simplify the implementation. This arithmetic deals with radix-10 ten’s complement integers of the form:

\[
Z = -s_z \times 10^d + \sum_{i=1}^{d} z_i \times 10^i,
\]

where \(d\) is the number of digits, \(s_z\) is the sign bit.
Parameter e is the excess of the representation and usually takes values 0 (non excess), 3 or 6. The redundancy index r is defined as $r \equiv m \_ l \_ r \_ l \_ r$ [12], being radix 10.

This binary encoding simplifies the hardware implementation of decimal arithmetic units, since we can make use of state-of-the-art binary logic and binary arithmetic techniques to implement digit operations. In particular, the ODDS representation presents interesting properties (redundancy and binary encoding of its digit set) for a fast and efficient implementation of multioperand addition. Moreover, conversions from BCD to the ODDS representation are straightforward, since the digit set of BCD is a subset of the ODDS representation.

An important issue for this representation is the ten’s complement operation. Since after the recoding of the multiplier digits, negative multiplication digits may result, it is necessary to negate (ten’s complement) the multiplicand to obtain the negative partial products. This operation is usually done by computing the nine’s complement of the multiplicand and adding a one in the proper place on the digit array.

3 High-Level Architecture

The high-level block diagram of the proposed parallel architecture for d _ d-digit BCD decimal integer and fixed-point multiplication is shown in Fig. 1. This architecture accepts conventional (non-redundant) BCD inputs X, Y , generates redundant BCD partial products PP, and computes the BCD product P¼ X _ Y . It consists of the following three stages1: (1) parallel generation of partial products coded in XS-3, including generation of multiplicand multiples and recoding of the multiplier operand, (2) recoding of partial products from XS-3 to the ODDS representation and subsequent reduction, and (3) final conversion to a non-redundant 2d-digit BCD product.

TABLE 1 Nine’s Complement for the XS-3 Representation 1. Each stage is explained in detail in the next sections, stage 1 in Section 4, stage 2 in Section 5, and stage 3 in Section 6. In particular, we provide implementations suited for the IEEE 754-2008 decimal arithmetic formats [15], that is, for d¼ 16 (Decimal64) and d¼ 34 digits

Fig. 1. Combinational SD radix-10 architecture.

Stage 1) Decimal partial product generation. A SD radix-10 recoding of the BCD multiplier has been used. This recoding produces a reduced number of partial products that leads to a significant reduction in the overall multiplier area [29]. Therefore, the recoding of the d-digit multiplier Y into SD radix-10 digits Ybd_1; . . . ; Yb0, produces d partial products PP½d _ 1_; . . . ; PP½d _ 0_, one per digit; note that each Ybk recoded digit is represented in a 6–bit hot-
one code to be used as control input of the multiplexers for selecting the proper multiplicand multiple, \( f_5X, \ldots, _1X; 0X; 1X; \ldots; 5Xg. \) An additional partial product \( PP_{2d} \) is produced by the most significant multiplier digit after the recoding, so that the total number of partial products generated is \( d + 1 \). In contrast to our previous SD radix-10 implementations, \( 3X \) is obtained in a reduced constant time delay (_3 XOR-gate delays) by using the XS-3 representation. Moreover, a negative multiple is generated from the correspondent positive one by a bitwise XOR operation. Consequently, the latency is reduced and the hardware implementation is simplified. The scheme proposed in also produces \( 3X \) in constant time but using redundant signed-digit BCD arithmetic.

Stage 2) Decimal partial product reduction. In this stage, the array of \( d + 1 \) ODDS partial products are reduced to two 2d-digit words (A, B). Our proposal relies on a binary carry save adder tree to perform carry-free additions of the decimal partial products. The array of \( d + 1 \) ODDS partial products can be viewed as adjacent digit columns of height \( h \geq d + 1 \). Since ODDS digits are encoded in binary, the rules for binary arithmetic apply within the digit bounds, and only carries generated between radix-10 digits (4-bit columns) contribute to the decimal correction of the binary sum. That is, if a carry out is produced as a result of a 4-bit (modulo 16) binary addition, the binary sum must be incremented by 6 at the appropriate position to obtain the correct decimal sum (modulo 10 addition).

4. Decimal Partial Product Reduction

The PPR tree consists of three parts: (1) a regular binary CSA tree to compute an estimation of the decimal partial product sum in a binary carry-save form (S, C), (2) a sum correction block to count the carries generated between the digit columns, and (3) a decimal digit 3:2 compressor which increments the carry-save sum according to the carries count to obtain the final double-word product (A;B), A being represented with excess-6 BCD digits and B being represented with BCD digits. The PPR tree can be viewed as adjacent columns of \( h \) ODDS digits each, \( h \) being the column height (see Fig. 4), and \( h \geq d + 1 \). Fig. 2 shows the high-level architecture of a column of the PPR tree (the \( i \)th column) with \( h \) ODDS digits in \([0, 15]\) (4 bits per digit). Each digit column of the binary CSA tree (the gray colored box in Fig. 2) reduces the \( h \) input digits and \( ncin \) input carry bits, transferred from the previous column of the binary CSA tree, to two digits, \( S_i, C_i \), with weight \( 10^i \). Moreover, a group of \( ncout \) carry outputs are generated and transferred to the next digit column of the PPR tree. Roughly, the number of carries to the next column is \( ncout = h - 2 \). The digit columns of the binary CSA tree are implemented efficiently using 4-bit 3:2, 4:2 and higher order compressors made of full adders. These compressors take advantage of the delay difference of the inputs and of the sum and carry outputs of the full adders, allowing significant delay reductions. The weight of the carry-outs generated at the \( i \)th column, \( cip_{1/20}; \ldots; cip_{1/2ncout - 1} \), is \( 16 \geq 10^i \) because the addition of the 4-bit digits is modulo 16. These carries are transferred to the \( d + 1 \)th column of the PPR tree, with weight \( 10^i \geq 1 \frac{1}{4} 10 \geq 10^i \). Thus, there is a difference between the value of the carry
outs generated at the i-column and the value of the carries transferred to the \((i \, \mid \, 1)\)-column. This difference, \(T\), is computed in the sum correction block of every digit column and added to the partial product sum \((S, C)\) in the decimal CSA.

![Fig. 2 High-level architecture of the proposed decimal PPR tree (h inputs, 1-digit column).](image)

**CONCLUSION**

In this paper we have presented the algorithm and architecture of a new BCD parallel multiplier. The improvements of the proposed architecture rely on the use of certain redundant BCD codes, the XS-3 and ODDS representations. Partial products can be generated very fast in the XS-3 representation using the SD radix-10 PPG scheme: positive multiplicand multiples \((0X, 1X, 2X, 3X, 4X, 5X)\) are precomputed in a carry-free way, while negative multiples are obtained by bit inversion of the positive ones. On the other hand, recoding of XS-3 partial products to the ODDS representation is straightforward. The ODDS representation uses the redundant digit-set \([0, 15]\) and a 4-bit binary encoding (BCD encoding), which allows the use of a binary carry-save adder tree to perform partial product reduction in a very efficient way. We have presented architectures for IEEE-754 formats, Decimal64 (16 precision digits) and Decimal128 (34 precision digits). The area and delay figures estimated from both a theoretical model and synthesis show that our BCD multiplier presents 20-35 percent less area than other designs for a given target delay.

5. Experimental result

![Fig 3 : simulation wave form of 16x16 multiplier](image)
Fig 4: RTL schematic of 16x16 multiplier

REFERENCE


Improve Unbalanced Dc Sources by Using Netural Voltage Modulation in Multilevel Inverters

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Abstract: This specific project offers a pulse width-modulation technique to achieve balanced line-to-line output voltages and maximize this modulation index inside the linear modulation range the place that the output voltage could be linearly adjusted inside the multilevel cascaded inverter (MLCI) running under unbalanced dc-link conditions. Here we are implementing seven level cascade inverter. In these conditions, this linear modulation variety is lowered, and an important output voltage difference may happen as voltage references increase. So that you can analyze these effects, the voltage vector living space for MLCI can be evaluated in depth. From this analysis, the theory behind this output voltage difference is defined, and the ideal linear modulation variety considering the unbalanced dc-link problem is evaluated. After that will, a neutral voltage modulation tactic is proposed to obtain output voltage balancing and also to lengthen the linear modulation range around the greatest reachable point theoretically. In this proposed method, too large of any dc-link difference precludes this balancing of the output voltages. This limitation is also discussed. Both this simulations plus the experiments for just a seven-level phase shifted modulated MLCI pertaining to electric vehicle traction engine drive show that the proposed method will be able to balance line-to-line productivity voltages and also to maximize the linear modulation range beneath unbalanced dc-link disorders.

Index Terms
Harmonic injection, multilevel cascaded inverters (MLCIs), neutral voltage modulation (NVM), phase-shifted (PS) modulation, space vector pulse width modulation (PWM) (SVPWM).

1 Introduction
Multilevel inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low \( \frac{dv}{dt} \) characteristics and generally have low harmonics in the output voltage and current. In addition, the switching of very high voltages can be achieved by stacking multilevel inverter modules [1]–[3]. Due to these advantages, multilevel inverters have been applied in various application fields [6]–[10]. Among various topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one of the prominent topologies because of its simple structure for modularization and fault-tolerant capability.

Therefore, MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction
drives, In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods. Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives, where dynamic properties are very important, whereas SHEPWM is preferred in some high-power static power conversion applications. An SVPWM method has been studied to cover the over modulation range in the multilevel inverter. To reduce the common-mode voltage, a multilevel SVPWM has been proposed in. The series SVPWM method has been reported to easily implement SVPWM for the MLCI an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency.

In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range are easily obtained through simple arithmetic calculations. In the proposed method, too large of a dc-link imbalance precludes the output voltages from being balanced. This limitation is also discussed. In addition, a fault-tolerant operation is naturally covered, because the MLCI undergoing an unbalanced dc-link condition can be considered as an MLCI operating under a faulty condition on switch modules.

Compared to the existing methods, the proposed strategy is very simple to implement, compensates the output voltage imbalance in real time, and maximizes the voltage utilization of the dc links. Therefore, if this scheme is applied to applications such as EV traction drive systems, the dynamic characteristics can be greatly improved. This paper is organized as follows. In Section II, the voltage vector space for the one-by-three configuration MLCI is analyzed for a conceptual study.

2. MULTILEVEL INVERTER

In response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter.

As reported in the literature, the H-bridge cascade inverter has been used in several practical instances for broadcasting amplifier [4], plasma [3], industrial drive [6] as well as STATCOM [7] applications etc. The main limitation of the H-bridge cascade inverter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. For STATCOM application, where the isolated supplies are not required, the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates over-sizing of the dc link capacitors.

The capacitor clamping inverter, though the three-level scheme of which was published in the early 1980’s [8], had been rarely discussed until the introduction of the “imbricated cells” [9]. The individual
clamping capacitor needs only to smooth the switching frequency ripple voltage and the required capacity for each clamping capacitor is therefore small. However, as the number of level increases, such problems as thermal designing, low-inductance designing, as well as insulation designing of the system will become critical. Medium voltage drives using four-level capacitor clamping inverter has recently been available on the market.

The diode clamping inverter, as shown in Fig. 4.1, published by different researchers in the early 90’s can be deemed as the extension of the neutral-point-clamped (NPC) inverter introduced in the early 80’s. Unlike the NPC inverter which has been extensively used today in industrial drives, tractions as well as FACTS systems, the diode clamping inverter is right under investigation.

In addition to the dc link unbalance problem identified in the other problems with the diode clamping inverter.

3.PROPOSED MODULATION TECHNIQUE

the maximum synthesizable voltage in the linear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

3.1 Traditional Offset Voltage Injection Method

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load [43], [44]. For example, the offset voltage $v_{sn}$ is injected to the phase voltage references $v_{as}$, $v_{bs}$, and $v_{cs}$ to implement carrier-based SVPWM as in

$$
v_{sn} = \frac{v_{\text{max}} + v_{\text{min}}}{2}, \quad v_{\text{max}} = \max (v_{as}, v_{bs}, v_{cs}), \quad v_{\text{min}} = \min (v_{as}, v_{bs}, v_{cs}).
$$

Then, the pole voltage references $v_{an}$, $v_{bn}$, and $v_{cn}$, which will be converted to PWM duty references, are

$$
v_{an} = v_{as} - v_{sn}, \quad v_{bn} = v_{bs} - v_{sn}, \quad v_{cn} = v_{cs} - v_{sn}.
$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2 Proposed NVM Method

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches Vph_max. This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage reference in the linear modulation range, the other phases can be saturated or go into the overmodulation region. In this situation, a neutral voltage can be produced by the saturated or overmodulated phase.
In order to resolve this issue and to synthesize the output voltage to $V_{\text{ph}_{\text{max}}}$ in the linear modulation range, the NVM technique is proposed in this paper. Fig. 3.1 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points $n$ and $s$ in Fig. 3.1 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant $K_w$ is defined as

$$K_w = \frac{V_{\text{de}_{\text{mid}}} + V_{\text{de}_{\text{min}}}}{2}.$$ 

By using (12), the weight factors are calculated as

$$K_{w_a} = \frac{V_{\text{de}_{\text{a}}}}{K_w}, \quad K_{w_b} = \frac{V_{\text{de}_{\text{b}}}}{K_w}, \quad K_{w_c} = \frac{V_{\text{de}_{\text{c}}}}{K_w},$$

where $K_{w_a}, K_{w_b},$ and $K_{w_c}$ represent the weight factors for phases $a, b,$ and $c,$ respectively. Next, the weight factors are multiplied by the phase voltage references, and the new references $v_{\text{as}}, v_{\text{bs}},$ and $v_{\text{cs}}$ are obtained as

$$v_{\text{as}}' = K_{w_a}v_{\text{as}}, \quad v_{\text{bs}}' = K_{w_b}v_{\text{bs}}, \quad v_{\text{cs}}' = K_{w_c}v_{\text{cs}}.$$

It should be noted that, depending on dc-link conditions, the sum of $v_{\text{as}}, v_{\text{bs}},$ and $v_{\text{cs}}$ may not be zero. By using these components, the injected voltage $v_{\text{sn}}$ and the pole voltage references are given as

$$v_{\text{sn}}' = \frac{v_{\text{max}} + v_{\text{min}}}{2} = \frac{v_{\text{a}}' - v_{\text{a}}' + v_{\text{b}}' - v_{\text{b}}' + v_{\text{c}}' - v_{\text{c}}'}{3}.$$ (15)

From (13), the line-to-line voltages across each phase of the load are represented as

$$\left[ \begin{array}{c} v_{\text{a}}' \\ v_{\text{b}}' \\ v_{\text{c}}' \end{array} \right] = \left[ \begin{array}{ccc} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{array} \right] \left[ \begin{array}{c} v_{\text{a}} 
 v_{\text{b}} 
 v_{\text{c}} \end{array} \right] = \left[ \begin{array}{c} v_{\text{a}} - v_{\text{b}} + v_{\text{c}} \\ v_{\text{a}} - v_{\text{c}} + v_{\text{b}} \\ v_{\text{b}} - v_{\text{c}} + v_{\text{a}} \end{array} \right].$$ (16)

As it can be seen in (16), $v_{\text{sn}}$ does not appear in the line-to-line voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors $K_{w_a}, K_{w_b},$ and $K_{w_c},$ which are inversely proportional to the corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$|V_{\text{de}_{\text{a}}} < V_{\text{de}_{\text{b}}} < V_{\text{de}_{\text{c}}}.|$$

Then, from (13) and (17)

$$K_{w_a} > K_{w_b} > K_{w_c}, \quad K_{w_a} > 1, \quad K_{w_b}, K_{w_c} < 1.$$ (17)

Equation (18) gives

$$|v_{\text{a}}'_{\text{as}} < |v_{\text{a}}'_{\text{bs}} < |v_{\text{a}}'_{\text{cs}} < |v_{\text{a}}'_{\text{as}}|.$$ (19)

From (13) and (19), it can be recognized that, if $v_{\text{as}},$ whose dc-link
voltage is less than the others, is corresponding to \( v_{\text{max}} \) or \( v_{\text{min}} \), the absolute value of \( v_{\text{sn}} \) is greater than \( v^*_{\text{sn}} \) in (10). On the other hand, the final pole voltage references \( v^*_{an}, v^*_{bn}, \) and \( v^*_{cn} \) are calculated by subtracting \( v_{sn} \) from the original phase voltage references \( v^*_{as}, v^*_{bs}, \) and \( v^*_{cs} \) as in (13). From this reasoning, in this example, it is supposed that, if \( v_{as} \) is corresponding to \( v_{\text{max}} \), then the final pole voltage references \( v^*_{an}, v^*_{bn}, \) and \( v^*_{cn} \) are less than the original pole voltage references \( V_{\text{dc}}, V_{\text{dc}_b} = V_{\text{dc}}, \) and \( V_{\text{dc}_c} = V_{\text{dc}}. \) which are not considering \( v_{\text{sn}} \) but \( v^*_{\text{sn}}. \) On the contrary, if \( v_{cs} \) is \( v_{\text{max}} \), then the final pole voltage references are greater than the original pole voltage references. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in (16), \( v_{\text{sn}} \) does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that \( V_{\text{dc}_a}, V_{\text{dc}_b}, \) and \( V_{\text{dc}_c} \) are equal to \( V_{\text{dc}} \)

\[
V_{\text{dc mid}} = V_{\text{dc min}} = V_{\text{dc}}.
\]

By substituting (20) into (12)–(14)

\[
K_{w} = \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{2} = V_{\text{dc}}.
\]

\[
K_{w_{a} = K_{w_{b} = K_{w_{c} = 1}}}
\]

\[
v'_{as} = v_{as},\ v'_{bs} = v_{bs},\ v'_{cs} = v_{cs}.
\]

Equation (21) shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

3.3 Constraints of the Proposed Method

In this section, the limitation of how unbalanced dc links can be while still being compensated by the proposed method is evaluated. Fig. 3.2 shows the modulated voltage waveforms with different modulation methods and dc-link conditions. In the figure, cases I and II show the results of traditional sinusoidal PWM (SPWM) and carrier-based SVPWM, while cases III and IV illustrate the waveforms of the proposed method with different ratios of dc-link voltages. The fundamental idea to examine the limitation of the proposed method is to evaluate what conditions bring the different polarities between the original voltage reference and the modified voltage reference by using the proposed method. In Fig.3.2, the vertices at \( \pi/2 \) and \( 3\pi/2 \) rad almost come in contact with, but do not cross, the zero
point. However, the directions of the vertices are opposite the original phase voltage reference in case IV. This means that an excessive and unnecessary voltage is injected into the system. As a result, the maximum linear modulation range is reduced, and the line-to-line voltage may be distorted. With this basic concept, it is assumed that a phase which has the lowest dc-link voltage commands $v^*_{\text{max}}$ and a phase which has the highest dc-link voltage commands $v^*_{\text{min}}$ to examine a worst case situation. From (14) and (13), the following equations can be established:

$$v'_{\text{max}} = \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{2V_{\text{dc min}}} v^*_{\text{max}}$$

$$v'_{\text{min}} = \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{2V_{\text{dc max}}} v^*_{\text{min}}$$

$$v'_{\text{st}} = \frac{v'_{\text{max}} + v'_{\text{min}}}{2}.$$

By using (22), the pole voltage reference which is considered as the worst case is

$$v^*_{\text{max, n}} = v^*_{\text{max}} - \frac{v'_{\text{max}} + v'_{\text{min}}}{2}.$$

By substituting (22) into (23), we have

$$v^*_{\text{max, n}} = \left(1 - \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{4V_{\text{dc min}}} \right) v^*_{\text{max}} - \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{4V_{\text{dc max}}} v^*_{\text{min}}.$$

Unless all three-phase voltage references are not zero simultaneously, near a positive peak of the original voltage reference, the sufficient condition which guarantees the same polarity between $v^*_{\text{max}}$ and $v^*_{\text{min}}$ is established as follows:

$$k_1 v^*_{\text{max, n}} > 0 \quad v^*_{\text{max}} > 0 \quad v^*_{\text{min}} < 0.$$

By substituting (24) into the first condition in (23), the following condition can be written:

$$k_1 = 1 - \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{4V_{\text{dc min}}}, \quad k_2 = \frac{V_{\text{dc mid}} + V_{\text{dc min}}}{4V_{\text{dc max}}}. \quad (26)$$

Here, it is obvious that $k_2$ is always positive. Therefore, as long as $k_1$ is positive, the condition (26) is always satisfied, and $k_1$ can be rearranged as follows

$$k_1 = \left(\frac{3V_{\text{dc min}} - V_{\text{dc mid}}}{4V_{\text{dc min}}} \right).$$
Equation (28) is then directly obtained from (27) to ensure that \( k_1 \) will always be positive.

\[
|V_{dc_{min}}| > \frac{1}{3}V_{dc_{mid}}.
\]

Note that (28) is a sufficient condition to meet the conditions in (23) so that the proposed method can be applied. However, even if (28) is not satisfied so that \( k_1 \) is negative, there still is a chance to apply the proposed method. To deal with this situation, let us consider the relationship between \( v^*_{\text{max}} \) and \( v^*_{\text{min}} \) as follows at a positive peak point:

\[
v^*_{\text{max}} = -2v^*_{\text{min}}.
\]

By substituting (29) into (26), we have

\[-2k_1 > k_2.
\]

Since \( k_1 \) is negative in this case, the following condition is derived from (30);

\[
|k_1| < \frac{k_2}{2}.
\]

If the relationship between \( k_1 \) and \( k_2 \) is established as in (31), even if the provision in (28) is broken, the conditions in (23) are satisfied so that the proposed method can still be effective. Let us recall Fig. 6.2 again here. In the figure, the values of \( |k_1| \) and \( k_2/2 \) for case III are evaluated as 0.1391 and 0.1393, respectively. Although the difference between the two values is very small, (31) is still true with these values. For case IV, the values of \( |k_1| \) and \( k_2/2 \) are calculated as 0.3 and 0.3, respectively. In contrast to case III, (31) is no longer satisfied, and the directions of the vertices are opposite, as explained previously. From the analysis in this section, both the methods in (28) and (31) are successfully able to judge the availability of the proposed method. In terms of accuracy, the latter may give better results. However, in practice, the former may be useful to judge the operation of the proposed method because it is already dealing with an extremely worst case on its own and the calculation in real time is much simpler than (31).

### 3.4 Duty Calculation

In Fig. 3.1, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

\[
d^*_a = d^*_b = \ldots = d^*_N = \frac{V_{\text{min}}^{*a}}{V_{dc_{a}}},
\]

\[
d^*_b = d^*_b = \ldots = d^*_N = \frac{V_{\text{max}}^{*b}}{V_{dc_{b}}},
\]

\[
d^*_c = d^*_c = \ldots = d^*_N = \frac{V_{\text{max}}^{*c}}{V_{dc_{c}}},
\]

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 3.3. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

### 4. SIMULATION & RESULT

A simple one-by-three configuration MLCI model is built in Matlab Simulink. The three-phase RL load with \( R = 0.1\Omega \) and \( L = 1\text{mH} \) is employed. The dc-link voltages for each phase are \( V_{dc_{a}} = 0.3 \times 30 \text{ V}, V_{dc_{b}} = 0.73 \times 30 \text{ V}, \) and \( V_{dc_{c}} = 30 \text{ V} \). From (7), the maximum synthesizable phase voltage in linear is
The voltage references are given by

\[ v_{\alpha \beta}^* = V_{ph_{max}} \sin(100\pi t) \]
\[ v_{bo}^* = V_{ph_{max}} \sin(100\pi t - 2\pi/3) \]
\[ v_{co}^* = V_{ph_{max}} \sin(100\pi t + 2\pi/3) \]

Equation is applied to the modulators of the inverter in open loop. Fig. 11 compares the voltage vector spaces and the voltage trajectories in the \( \alpha-\beta \)-axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space. The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable. The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods. Fig. 4.2 shows the time-domain simulation results with the same simulation condition. From \( t = 0.0 \) s to \( t = 0.03 \) s, traditional SPWM is used. From \( t = 0.03 \) s to \( t = 0.1 \) s, traditional SVPWM is used. After \( t = 0.1 \) s, the proposed method is applied. When
traditional SPWM is applied, $v_{sn}$ is zero, and the pole voltage references are identical to the ones in (34). With traditional SVPWM, $v_{sn}$ is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM.

However, the duty reference of phase $a$, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in $v_{sn}$, and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the last section of the figure. Under traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link.

**CONCLUSION**

The NVM technique for MLCIs under unbalanced dc-link conditions has been proposed in this paper. Here we done seven level cascade inverter. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the proposed method.

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An Anti-Islanding Protection of Distributed Generation with Fuzzy Logic Controller

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Abstract: Because of the variety of distribution generation (DG) dimensions along with technology linking in order to distribution networks, along with the issues connected with out-of-step are shutting, anti-islanding has long been a worry in which no apparent solution is present. This particular cardstock offers an automobile terrain approach that had been recommended within the wording of an IEEE working team in guidelines regarding DG safeguard. The prototype process had been constructed making use of common distribution equipment along with a lso are better controller, and yes it had been tested within the utility’s distribution analyze series. Outcomes demonstrate how the anti-islanding detection time is around a routine for a longer time compared to the delay connected with request on the auto terrain. When the auto terrain had been put on, this DG had been shut off in 1 routine in above existing safeguard. The most effective is inherently salable, relevant to every one DG sorts, is configurable in order to different lso are shutting practices along with isn't going to call for more apparatus as well as settings adjustments for the producer’s internet site.

1. Introduction

The integration of distributed generator has grown over the past decade and some utilities have reached very high penetration levels. Despite this experience the debate between utilities and private producers still rages on a number of technical issues. Possibly the most contentious is that of anti-islanding protection, where a reliable high speed communication based transfer-trip scheme and a local passive approach that relies only on the measurements of the voltage waveform represent, respectively, the most conservative and most liberal approaches. The anti-islanding and line protection are the two fundamental protection requirements that need to be met by all distributed generation (DG) installations, as detailed in the DG interconnection standards. Line protection consists of being able to detect all faults on the distribution feeder to which the DG is connected, while not disconnecting for faults on an adjacent feeder. Generally over current relaying is sufficient to meet this requirement, although in power electronic based generators, other strategies may be necessary due to the limited contribution to short circuits by these installations.

Anti-islanding has been the subject of a number of studies. These approaches can be typically divided into the following two classifications: passive approaches (using the local measurements of voltage and current, and variables derived from using these quantities, to delineate between islanding and grid connected operation) and active approaches (whereby the DG perturbs either the grid voltage or frequency, an approach intended to be benign while the grid is present, and to destabilize the system when the substation is open. A third approach is in fact a variant on communication based approaches, whereby using thyristor valves connected to ground, a disturbance is periodically injected at the substation- its presence at the DG’s location indicates a normal condition, whereas its absence is indicative of an islanded grid. Wang et al. have also suggested these thyristor based devices for fault identification in. Similar to active islanding techniques, this approach could be criticized alone on the impact on power quality. Additionally, in noisy grids or feeders that are particularly long, the issue of nuisance tripping is an issue.

This paper proposes an approach to anti-islanding protection that is based on applying a three-phase short circuit to the islanded distribution system just prior to reclosing or reenergization. Section II provides the theory and methodology for construction of this utility-owned equipment. Section III presents the experimental set-up and results, and we conclude with a summary of various practical considerations.

1.2 Anti Islanding System

Islanding refers to the condition in which a distributed generator (DG) continues to power a location even though electrical grid power from the electric utility is no longer present. Islanding can be
dangerous to utility workers, who may not realize that a circuit is still powered, and it may prevent automatic re-connection of devices. For that reason, distributed generators must detect islanding and immediately stop producing power; this is referred to as anti-islanding. The common example of islanding is a grid supply line that has solar panels attached to it. In the case of a blackout, the solar panels will continue to deliver power as long as irradiance is sufficient. In this case, the supply line becomes an "island" with power surrounded by a "sea" of unpowered lines. For this reason, solar inverters that are designed to supply power to the grid are generally required to have some sort of automatic anti-islanding circuitry in them. In intentional islanding, the generator disconnects from the grid, and forces the distributed generator to power the local circuit. This is often used as a power backup system for buildings that normally sell their excess power to the grid.

Detecting an islanding condition is the subject of considerable research. In general, these can be classified into passive methods, which look for transient events on the grid, and active methods, which probe the grid by sending signals of some sort from the inverter or the grid distribution point. There are also methods that the utility can use to detect the conditions that would cause the inverter-based methods to fail, and deliberately upset those conditions in order to make the inverters switch off. A Sandia Labs Report covers many of these methodologies, both in-use and future developments. These methods are summarized below.

2. RENEWABLE ENERGY

Renewable energy is generally defined as energy that comes from resources which are naturally replenished on a human timescale such as sunlight, wind, rain, tides, waves, and geothermal heat. Renewable energy replaces conventional fuels in four distinct areas: electricity generation, air and water heating/cooling, motor fuels, and rural (off-grid) energy services. Based on REN21's 2014 report, renewable contributed 19 percent to our global energy consumption and 22 percent to our electricity generation in 2012 and 2013, respectively. Both, modern renewable, such as hydro, wind, solar and bio fuels, as well as traditional biomass, contributed in about equal parts to the global energy supply. Worldwide investments in renewable technologies amounted to more than US$214 billion in 2013, with countries like China and the United States heavily investing in wind, hydro, solar and bio fuels.

![Wind, solar, and biomass are three emerging renewable sources of energy](image1)

![Global public support for different energy sources (2011)](image2)

Renewable energy resources exist over wide geographical areas, in contrast to other energy sources, which are concentrated in a limited number of countries. Rapid deployment of renewable energy and energy efficiency is resulting in significant energy security, climate change mitigation, and economic benefits. In international public opinion surveys there is strong support for promoting renewable sources such as solar power and wind power. At the national level, at least 30 nations around the world already have renewable energy contributing more than 20 percent of energy supply. National renewable energy markets are projected to continue to grow strongly in the coming decade and beyond.

While many renewable energy projects are large-scale, renewable technologies are also suited to rural and remote areas and developing countries, where energy is often crucial in human development. United Nations' Secretary-General Ban Ki-moon has said that renewable energy has the ability to lift the poorest nations to new levels of prosperity.
Renewable energy flows involve natural phenomena such as sunlight, wind, tides, plant growth, and geothermal heat, as the International Energy Agency explains: Renewable energy is derived from natural processes that are replenished constantly. In its various forms, it derives directly from the sun, or from heat generated deep within the earth. Included in the definition is electricity and heat generated from solar, wind, ocean, hydropower, biomass, geothermal resources, and biofuels and hydrogen derived from renewable resources.

3. THEORY AND METHODOLOGY

3.1 Introduction

Anti-islanding protection is required of any distributed generator connecting to the distribution network, in order to protect against the case that the DG continues to energize the feeder when the utility has opened-creating an unintentional island. An unintentional island, although rather unlikely in real life, could be created by one of two scenarios. The first case is a result of the inadvertent opening of the substation feeder breaker/recloser or one of the protection devices further down the feeder. This could be done in error or as a planned operation where the utility personnel do not realize that there is a DG present on the line. Eventually the line is re-energized and the risk of out-of-phase reclosing exists, if the DG remains online. The second, even less likely situation would be a temporary fault that leads to operation of the utility protection device but the DG’s protection does not operate before the self-clearing fault extinguishes, creating the temporary island. For example, a tree branch might touch the line and it is cleared at the moment the vacuum bottle interrupter of a recloser operates. Although less likely, the latter of the two cases is generally used to define the anti-islanding requirements, which links the requirement to first period reclosing time of the local utility (2 s is given in IEEE 1547, the typical first operation reclosing time of many North American utilities, although some are as fast as 0.5 s). This defines the speed at which the DG’s anti-islanding protection must detect the island.

The solution proposed in the present work, termed an autoground, is seen as a compromise in terms of cost and performance between the transfer-trip and local passive measurements. Fig. 3.1 presents the autoground concept, where the autoground system is installed just downline of the utility protection device (substation breaker or inline recloser). In this configuration, following opening of the utility breaker, the autoground opens the substation side device, denoted sectionalizing switch (SS) and closes the autogrounding switch (AS) effectively applying a three phase to ground fault. All DGs that have not already disconnected will be forced to disconnect based on their anti-islanding protection requirements, which will be forced to disconnect based on line protection.
computerized sectionalizer capacities would be adequate. For applications where the autoground is combined with an in-line recloser, the SS is not needed as its usefulness can essentially be coordinated into the recloser itself. Fig. 4.2 represents the vacuum jug based recloser utilized as a part of the trial set-up as the SS. As the AS is joined in parallel with the dissemination organize just so as to apply the shortcoming, it doesn’t have to intrude on deficiency current either.

As a result, the apparatus is even simpler, and was realized by a slight modification to an automated capacitor bank assembly. The same vacuum bottle switches were used but with their secondary connected to the neutral conductor rather than capacitor banks (Fig.3.3). In this case, the switches were actuated by relays, controlled by a simple circuit housed at the base of the pole. This circuit was used to integrate outputs from the SEL-351 relay, installed at the base of the SS pole, and used to control both the SS and the AS. The SEL-351 was chosen for the experimental set-up but any relay used for control of distribution protection devices would likely suffice. Again, in the case that the inline recloser served also for the SS functionality, its controller would only need to be reprogrammed to output signals for the AS, installed on the adjacent pole. The next section defines the logic required in order to realize the autoground system’s functionality.

3.3 Control Logic

The sequence of events for an action of the autoground is illustrated in Fig. 3.4. Within this sequence, the control needs to perform three separate functions: coordinate opening of the sectionalizing switch with the upline protection device; application of autogrounding switch for a predetermined duration; and closing of the sectionalizing switch, again coordinated with the upline device. Implicit is

![Fig. 3.2. Autoground sectionalizing switch.](image)

![Fig. 3.3. System autogrounding switch apparatus: assembly (left) vacuum bottle](image)

![Fig. 3.5. Autoground sectionalizing switch closing and opening logic.](image)

![Fig. 3.6. Autoground closing and opening logic.](image)
an understanding of the reclosing strategy in place, as the design is meant to respond to the unintentional islanding cases created during a protection device action. Fig. 3.5 illustrates the connection of the controller to the network and the logic for opening and closing of the sectionalizing switch. It is proposed to detect the opening of the upline protection device using an undercurrent relay.

However, detecting a sufficiently small undercurrent on the three phases could not be done directly in the relay logic. Therefore, two alternatives were considered: using the complement of an overcurrent relay [NOT(50)] or convert the current to a voltage and use an undervoltage relay of the resulting signal. The latter was chosen as the 50 does not permit settings of less than 5 A on the medium voltage level (it is configured to measure large currents). Thus, the output of the CT was connected through an appropriate burden (to convert the current to a voltage signal) to the controller external inputs (Fig. 3.5). Applying these signals to an undervoltage relays (27) then enables detection of the undercurrent condition. The sequence of events is described here.

Upon opening of the upline breaker, an undercurrent is detected on the three phases (defined as 10% of the minimum load current on the line), signaling an opening operation of the SS. Even in the presence of distributed generation, zero current will never occur with the breaker closed, due to the inductive component of the line. Once the logic signal LT9 returns to zero (representing opening to a voltage signal) to the controller external inputs (Fig. 3.5). Applying these signals to an undervoltage relays (27) then enables detection of the undercurrent condition. The sequence of events is described here.

In the experimental set-up, the manual close was replaced simply by a counter, corresponding to just before the reclosing operation. Finally, the autogrounding switch is controlled by two logic circuits that then output the closing and opening pulses to two of the outputs, Fig. 3.6. These outputs are connected to the actuation circuit, installed at the base of the AS on the adjacent pole. As can be noted, the trip signal from the SS causes LT9 to change state, initiating a number of delayed step functions (SV3, SV4, SV8, and SV10). The combination of these steps through two flip-flops leads to two pulses of 30 cycles, at 100 and 600 cycles (1.67 and 10 s) from the opening of the upline breaker. These two pulses are respectively used to close and open the AS. Obviously, each of these times is configurable in order to be compatible with the utility’s reclosing practices and the disconnection time of the different DGs. The application time of the autoground, \( t \), must be compatible with the fault detection time of all DGs for a bolted fault (symmetrical or asymmetrical) at the autoground’s location. For example, if the protection study demonstrates that the DG will trip within 6 cycles for this case, must be longer than these 6 cycles. Otherwise, some form of voltage check must be integrated into the logic to ensure that all DGs have indeed disconnected prior to removal of the autoground.

3.4 Other Considerations

The previous section detailed the realization of the autoground system; however, there are a number of considerations prior to integration into a particular utility’s system. We discuss some of the most important ones here. The autoground system is there to serve as back-up anti-islanding protection to the DG’s passive settings; however, first and foremost it needs to be compatible with the distribution protection practices already in place. Logically, application of the autoground is only required for the first reclosing period, as the DG is required to remain disconnected for 5 min after tripping.

However, if different reclosing times are used and it is decided to apply the autoground during each period, the delays within the above logic need to be compatible with each of the reclosing periods. An autoground will be installed at each protection device (substation breaker, recloser) that is upline of the furthest DG along the feeder. For example, the DG might be installed downstream of two in-line reclosers, requiring three autogrounds (one for the substation breaker, and one for each recloser). In certain cases, if possible, it may be preferable to have a device moved in order to simplify coordination and limit the number of autoground systems that need to be installed. With regards to the autoground itself, the vacuum bottle switches are very reliable (rated for 1200 operations) but the design still needs to handle the case that it may fail to open.

This problem is taken care of by the selection of an appropriately rated fuse that would clear the phase that failed to operate upon reclosing of the system. Subsequent operation of the
autoground would then apply an asymmetrical fault, until the issue was identified and the fuse replaced. The selection of the fuses must be done in order to coordinate with the substation protection so that the fuse would blow before the substation protection operates. The time for which the autoground is applied, needs to take into account the line protection tripping time for all DGs.

Additionally, the fuses need to be appropriate selected so that the fuses will not blow when the fault is fed from the DGs. Obviously if a DG remains online until the operation of the autoground, it will be subjected to a fault and the resulting electromechanical stresses. This could be met with resistance from the DG proponent; however there are two arguments to address this issue. The first is that the application of the autoground can be timed to be towards the end of the reclosing period, providing ample time for the DG to detect the islanding condition and disconnect. Secondly, the DG needs to be designed in order to handle these types of fault anyways so it is a bit of a non-issue, although the frequency of faults may be slightly increased.

4. FUZZY CONTROLLER

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection. To understand why use of fuzzy logic has grown, we must first understand what is meant by fuzzy logic.

Fuzzy logic has two different meanings. In a narrow sense, fuzzy logic is a logical system, which is an extension of multivalve logic. However, in a wider sense fuzzy logic (FL) is almost synonymous with the theory of fuzzy sets, a theory which relates to classes of objects with unsharp boundaries in which membership is a matter of degree. In this perspective, fuzzy logic in its narrow sense is a branch of FL. Even in its more narrow definition, fuzzy logic differs both in concept and substance from traditional multivalve logical systems.

In fuzzy Logic Toolbox software, fuzzy logic should be interpreted as FL, that is, fuzzy logic in its wide sense. The basic ideas underlying FL are explained very clearly and insightfully in Foundations of Fuzzy Logic. What might be added is that the basic concept underlying FL is that of a linguistic variable, that is, a variable whose values are words rather than numbers. In effect, much of FL may be viewed as a methodology for computing with words rather than numbers. Although words are inherently less precise than numbers, their use is closer to human intuition. Furthermore, computing with words exploits the tolerance for imprecision and thereby lowers the cost of solution.

5. SIMULATION AND RESULTS

The testing was conducted on IREQ’s distribution test line, configured according to Fig. 5.1. The autoground system was installed at the end of the first feeder. The synchronous generator was connected to the second feeder through a 500 V/25 Kv transformer, as indicated. The parameters of the synchronous generator and the overcurrent protection are provided in the Appendix. Switches on feeders 2 and 3 were opened in order to feed them both from feeder 1. The testing consisted of first synchronizing the generator, balancing its output power with the 150 kW load and then initiate opening of the SS for three different configurations of the autoground: with all three fuses in service; with one fuse removed; and with two of the three fuses removed. Synchronized data was acquired using the LX-TEAC data acquisition system, monitoring the following parameters: threephase currents and voltages at 25 kV (point 1), 500 V (point 2) and the generator torque (point 3). Additionally, measurement of the ground voltage at 1 m, 5 m and 75 m (taken to be the zero reference) was performed in order to investigate the earth voltage rise during operation of each of the cases.

Fig. 5.1. IREQ distribution test line configuration for autoground testing.
Fig. 5.2. Substation voltages (top) and currents (bottom) during opening of SS and application of the AS.

Fig. 5.3. Current waveforms of the synchronous generator during application of the autoground.

Fig. 5.4. Three phase voltages (top) and currents (bottom) of synchronous generator during opening of SS and application of the autoground.

Fig. 5.5. Torque measurement on the synchronous generator shaft during test (expressed on the base of the real power prior to the islanding event).

Extension results with fuzzy logic controller

Fig. 5.6. Substation voltages (top) and currents (bottom) during opening of SS and application of the AS.

Fig. 5.7. Three phase voltages (top) and currents (bottom) of synchronous generator during opening of SS and application of the autoground.

Fig. 5.8. Current waveforms of the synchronous generator during application of the autoground.
CONCLUSIONS

This paper has conferred a climbable, low price approach for anti-islanding protection of distributed generation, employing a utility closely-held associated operated system remarked as an autoground. The planning of the system and its management were conferred and a epitome system was created victimisation commonplace distribution utility instrumentation. Testing results were conferred for symmetrical and asymmetrical operation of the system. Altogether cases, the DG’s over current protection isolated the generator from the system in but 2 cycles. The height force determined exceeded momentarily around four times the pre-fault price. The results valid the thought for one generator supported a synchronous machine, whereas future work can study its pertinence to systems with massive numbers of decigram, as well as those with power electronic interfaces. The answer shows promise as a result of its comparatively low price and inherent quantifiability.

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Control of a Hybrid Multilevel Converter with Floating DC-links for Current Waveform Improvement

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Abstract: Multilevel converters offer advantages in terms of the output waveform quality due to the increased number of levels used in the output voltage modulation. This advantage is particularly true for cascaded H-bridge converters that can be built to produce a large number of levels thanks to their modular structure. Nevertheless, this advantage comes at the cost of multiple DC-links supplied by independent rectifiers through the use of a multi-output transformer for inverters. This frontend complicates the implementation of converters that have a high number of levels. An alternative method of using lower voltage cells with floating dc-links to compensate only for voltage distortion of an NPC converter is considered for active rectifier applications. The analogy between the floating H-bridges and series active filters is used to develop a strategy for harmonic compensation of the NPC output voltage and the control of the floating dc-link voltages. This simplifies the current control scheme and increases its bandwidth. Simulation results with a low power prototype that show the good performance of the proposed modulation technique and the resulting improvement in the output waveform are provided.

1 Introduction

In the last decade, medium-voltage high-power converters have become widely used as drives for pumps, fans and material transport in a number of industries, as well as for VAR compensation in grid applications. At this voltage range, multilevel converters are preferred to overcome the voltage blocking limitations of the available switches. Another important advantage of this technology is the improved output waveforms due to the higher number of levels in the output voltage waveform, compared to the conventional three-phase two-level inverter. Similarly, an increased number of voltage levels will result in a reduced input filter size for grid connected applications. Moreover, a high number of levels allow the device switching frequency to be reduced for a given current distortion.

The multilevel topologies can be classified into three main categories: the neutral point clamped (NPC), the flying capacitors (FC), and the cascaded H-bridge (CHB) converters. The three level NPC bridge is probably the most widely used topology for medium voltage AC motor drives and PWM active rectifiers. NPC converters with more levels are also possible, although there are significant problems in the balancing of their dc-link capacitor voltages, unless modified modulation strategies or additionally circuitry are used. On the other hand, the CHB converter is normally implemented with a large number of levels, but at the cost of complicated and bulky input transformers with multiple rectifiers or multi-winding three-phase output transformers. For this reason, in applications with no active power transfer, such as in reactive power compensation, where the converter can operate without the rectifier front-end, the CHB is a highly attractive solution.

In recent years an increased interest has been given to hybrid topologies integrating more than one topology in a single converter. Some authors have proposed the use of cascaded H-bridges fed by multilevel dc-links generated which are implemented with another converter topology. In a hybrid configuration based on the combination of an active NPC and a flying capacitor cell has been proposed to implement a five level converter. An hybrid converter formed by the series connection of a main three-level NPC converter and auxiliary floating H-Bridges (NPC-HBs) has been presented in.

In this topology, the NPC is used to supply the active power while the HBs operate as series active filters, improving the voltage waveform quality by only handling reactive power. In this way,
this topology reduces the need for bulky and expensive LCL passive filters, making it an attractive alternative for large power applications. In this work, the control strategy for the NPC-HBs hybrid converter, previously introduced in, is experimentally verified. This includes: low frequency synchronous modulation of the NPC and the generation of the HBs voltage references for dc-link voltage control.

2.HYBRID MULTILEVEL CONVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were “inverted”, to convert DC to AC. The inverter performs the opposite function of a rectifier.

3.Neutral Point Clamped (NPC) Inverters

NPC converters also known as three-level inverters. Problems of 2-level inverter in high-power applications.High DC link voltage requires series connection of devices.Difficulty in dynamic voltage sharing during switching. These problems are solved by using NPC inverter or multilevel inverter. The below Fig 3.6 shows the NPC inverter circuit.

Fig 3.1 NPC inverter
DC link capacitor split to create neutral point 0, Q11, Q14 : main devices (2-level inverter), Q12, Q13 : auxiliary devices – clamp output potential to neutral point with help of clamping diodes D10, D10’. Apply all PWM techniques. Consider HEPWM technique to eliminate 2 lowest significant harmonics (5th and 7th) and control fundamental voltage. Phase voltage waveform (v_0) and corresponding gate signals. Each output potential clamped to neutral potential in off periods of PWM control.

For positive phase current +ia,
Q11, Q12 : when v_0 positive
D13, D14 : when v_0 negative
D10, Q12 : at neutral clamping condition
For negative phase current -ia,
D11, D12 : when v_0 positive
Q13, Q14 : when v_0 negative
O13, D10’ : at neutral clamping condition.

- Operation mode gives :3 levels waveform for phase voltage (v_0) \rightarrow +0.5 Vd, 0, -0.5 Vd
- Levels of line voltage (v_{ab}) waveform of \rightarrow +Vd, -Vd, +0.5 Vd, -0.5 Vd and 0.
- Prove that each device has to withstand 0.5 Vd voltage.
- Each leg has 3 switching states.

State A : Upper switches ON.
State B : Lower switches ON.
State C : Auxiliary switches ON.

- Available switching states = 3^3 = 27 (8 for two-level inverters).

Advantages of npc converter are Allows voltage clamping. Improve PWM harmonic quality. Based on HEPWM technique, lower significant harmonics of NPC inverter attenuated considerably compared to two-level inverter Can be extended to more voltage levels for higher voltage/power levels. AS WELL dis advantages are extra devices required Fluctuation of neutral point voltages with finite size of DC link capacitors (voltage level redundancies permits manipulation of PWM signals without diminishing quality).Npc mainly used in Multi Megawatt
induction /synchronous motor drives for industrial applications.

4. Modeled Case Study Hybrid Topology

4.1 Power Circuit

The considered hybrid topology is composed by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase. The power circuit is illustrated in Fig. 4.2, with only the H-bridge of phase a shown in detail. For testing as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, arranged in a twelve-pulse configuration. The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy.

In the hybrid topology, the NPC inverter provides the total active power flow. For high-power medium voltage NPC, there are advantages to using latching devices such as IGCTs rather than IGBTs, due to their lower losses and higher voltage blocking capability imposing a restriction on the switching frequency. In this work, an NPC operating at a low switching frequency (of 250 Hz) is considered. In contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of IGBT.

The proposed converter, shown in Fig. can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, achieved by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC bridge is to be modulated at a low switching frequency, as proposed in this work, the second interpretation would seem to be more appropriate to devise a control algorithm, leading to the following two design challenges:

- To determine the lowest value of H-bridge dc-link voltage (VH) that achieves adequate voltage harmonic compensation.
- To devise a control algorithm that ensures that the floating dc-links are properly regulated at this value.

For the modulation of the NPC inverter, the Selective Harmonic Elimination (SHE) method has been selected. This method has the advantage of very low switching frequency and hence low switching losses, while eliminating the low order harmonics. With the use of SHE modulation, the fundamental output voltage of the converter is synthesized by the NPC converter and thus the series HBs will only need to supply reactive power, allowing for operation with floating capacitor DC-links.

A drawback of any synchronous modulation method, such as SHE, is its limited dynamic capability and poor closed loop performance due to the use of a pre-calculated lookup table based approach, rather than real time calculations. These drawbacks can, to a large extent, be overcome by the use of the series H-bridges which are modulated in real time, introducing an additional degree of control freedom to the circuit and cleaner feedback signals.

5. Simulation and Results

The first phase of the work was to evaluate the proposed topology and control method. Experimental results are included to show the
controlled DC-link voltage of the H-Bridges and the current waveform improvement for the Hybrid Inverter. A second stage with simulation results showing the proposed converter operating as AFE rectifier, using Matlab/Simulink coupled with the circuit simulator PSIM are also included. The physical ratings of the considered converter are those of a 1kW laboratory prototype with a total DC-link voltage of Vdc = 180V and rated current of 10A. The capacitors used for the H-bridges are CH = 2200 F and their reference voltages have been set to v_H = 30V.

![Fig 5.1 NPC topology power circuit](image1)

![Fig 5.2 NPC inverter operation at 50Hz with m = 0.8](image2)

Fig 5.1 NPC topology power circuit

Fig 5.2 NPC inverter operation at 50Hz with m = 0.8

Fig 5.3 Current spectrum for 50Hz operation with m = 0.8 NPC modulated by SHE.

The control platform for this type of a DSP board with a Texas Instrument TMS320C6713 processor coupled with a daughter board based on a Xilinx/Spartan III FPGA including multiple A/D converters. In this configuration, the FPGA operates as a sampling clock, triggering the A/D conversions and interrupting the DSP. The processor is used for the calculation of all the controllers which results in a voltage reference for the converter, with this voltage reference the processor addresses the SHE tables and passes the information of commutation angles (x and voltage phase to the FPGA. The FPGA performs the SHE modulation, the calculation of the harmonic references for the H-bridges and its unipolar PWM modulation using a carrier frequency of 2kHz.

![Fig 5.4 Hybrid topology power circuit](image3)

![Fig 5.5 Hybrid inverter operation at 50Hz with m = 0.8](image4)

Fig 5.4 Hybrid topology power circuit.

Fig 5.5 Hybrid inverter operation at 50Hz with m = 0.8.
CONCLUSION

This paper presents the series connection of a SHE modulated NPC and H-bridge multilevel inverter with a novel control scheme to control the floating voltage source of the H-bridge stage. The addition of the H-bridge series active filter or additional converter stage is not intended to increase the power rating of the overall converter. Rather, the main goal is to improve, in a controllable or active way, the power quality of the NPC Bridge which may have a relatively low switching frequency.

This enables superior closed loop performance for medium-voltage NPC-SHE based schemes. Where this modulation strategy has been selected for efficiency purposes it also allows the use of smaller inductive filters when connecting to the utility supply in AFE applications. Since no changes are made to the power circuit and modulation stage of the NPC inverter, the series H-bridge power circuit and its control scheme can be easily added as an upgrade to existing NPC driven applications.

The proposed series H-bridge filter control scheme can be used either as a grid or load interface, depending on whether the NPC converter is used as an AFE or inverter respectively. Both possibilities can be combined if used in a back to back configuration. The proposed floating dc-link voltage control scheme can be adapted to other hybrid topologies or cascaded H-bridge converters with the advantage that isolated input transformers can be avoided.

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Improve Dynamic Response For Fault Current Characteristics Of The DFIG With Fuzzy Logic Controller

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Abstract: In the recent times, due to environmental concerns, there is rapid growth of wind power in the electric power systems. Power system planners and operators are facing many difficulties while integrating wind power because of its inherent characteristics. To solve these difficulties there is need for various studies and models of wind turbines. Doubly Fed Induction Generator (DFIG) based Wind Turbine (WT) is one of the most popular configurations being adapted the proposed analysis method is applicable for the study of fault current characteristics of DFIG with different control strategies for low-voltage ride through. The research results are helpful to the construction of adequate relaying protection for the power grid with penetration of DFIGs. Her we can implement with fuzzy logic for better result.

Index Terms: Doubly fed induction generator (DFIG), dynamic response, fault current characteristics, non severe fault

I. INTRODUCTION

Due to environmental concerns caused by excessive exploitation of conventional resources, now the focus is diverted to non renewable resources especially solar & wind as these are environmentally clean and eco-friendly. With the modern technology incorporated in the wind turbines, wind power generation limits have been uplifted to considerable level in the grid. Hence penetration level of wind power has become more significant and is leading to more complex, sophisticated and reliable interconnection requirements. According to the requirements, dynamic behavior of grid should not get affected by operation of wind farm. But when grid is attributed to fault and voltage dips, the disconnection of the wind farm creates shedding of loads resulting in unreliable power supply. Therefore according to the magnitude of voltage at point of interconnection, the fault ride through capability is specified to withstand voltage dips without load shedding. Some more areas in which constraints need to be incorporated in study are power quality problems, protection of hardware equipments and ancillary services. To study these issues, dynamic model of WT has been developed. For the present study DFIG WT is considered. This WT is connected to grid through step up transformer. The Grid Side Converter and Rotor Side Converter are connected back to back to control generator output parameters in both normal & abnormal conditions. The Rotor Side Converter is current controlled & Grid Side Converter is voltage controlled. Both control schemes are based on per unit system. In these schemes, stationery frame is converted to synchronous frame and vice-versa. In synchronous frame, steady state or DC values are compared to desired references to achieve required output in synchronous frame. Apart from this crowbar protection circuit is also added so as to control over-current phenomenon in Rotor Side Converter which may arise in fault conditions.

II. FAULT CHARACTERSTICS

2.1 Introduction

In an electric power system, a fault is any abnormal electric current. For example, a short circuit is a fault in which current bypasses the normal load. An open-circuit fault occurs if a circuit is interrupted by some failure. In three-phase systems, a fault may involve one or more phases and ground, or may occur only between phases. In a "ground fault" or "earth fault", charge flows into the earth. The prospective short circuit current of a fault can be calculated for power systems. In power systems, protective devices detect fault conditions and operate circuit breakers and other devices to limit the loss of service due to a failure. In a poly phase system, a fault may affect all phases equally which is a "symmetrical fault". If only some phases are affected, the resulting "asymmetrical fault" becomes more complicated to analyze due to the simplifying assumption of equal current magnitude in all phases being no longer applicable. The analysis of this type of fault is often simplified by using methods such as symmetrical components.

2.2 Transient fault

A transient fault is a fault that is no longer present if power is disconnected for a short time and then restored; or an insulation fault which only temporarily affects a device's dielectric properties which are restored after a short time. Many faults in overhead power lines are transient in nature. When a fault occurs, equipment used for power system protection operates to isolate the area of the fault. A transient fault will then clear and the power-line can be returned to service. Typical examples of transient faults include:

- momentary tree contact
- bird or other animal contact
- lightning strike
- conductor clashing
Transmission and distribution systems use an automatic re-close function which is commonly used on overhead lines to attempt to restore power in the event of a transient fault. This functionality is not as common on underground systems as faults there are typically of a persistent nature. Transient faults may still cause damage both at the site of the original fault or elsewhere in the network as fault current is generated.

2.3 Persistent fault

A persistent fault does not disappear when power is disconnected. Faults in underground power cables are most often persistent due to mechanical damage to the cable, but are sometimes transient in nature due to lightning.

2.4 Symmetric fault

A symmetric or balanced fault affects each of the three phases equally. In transmission line faults, roughly 5% are symmetric. This is in contrast to an asymmetrical fault, where the three phases are not affected equally.

2.5 Asymmetric fault

An asymmetric or unbalanced fault does not affect each of the three phases equally. Common types of asymmetric faults, and their causes:

- line-to-line - a short circuit between lines, caused by ionization of air, or when lines come into physical contact, for example due to a broken insulator.
- line-to-ground - a short circuit between one line and ground, very often caused by physical contact, for example due to lightning or other storm damage
- double line-to-ground - two lines come into contact with the ground (and each other), also commonly due to storm damage.

2.6 Bolted fault

One extreme is where the fault has zero impedance, giving the maximum prospective short-circuit current. Notionally, all the conductors are considered connected to ground as if by a metallic conductor; this is called a "bolted fault". It would be unusual in a well-designed power system to have a metallic short circuit to ground but such faults can occur by mischance. In one type of transmission line protection, a "bolted fault" is deliberately introduced to speed up operation of protective devices.

2.7 Realistic faults

Realistically, the resistance in a fault can be from close to zero to fairly high. A large amount of power may be consumed in the fault, compared with the zero-impedance case where the power is zero. Also, arcs are highly non-linear, so a simple resistance is not a good model. All possible cases need to be considered for a good analysis.

2.8 Arcing fault

Where the system voltage is high enough, an electric arc may form between power system conductors and ground. Such an arc can have relatively high impedance (compared to the normal operating levels of the system) and can be difficult to detect by simple over current protection. For example, an arc of several hundred amperes on a circuit normally carrying a thousand amperes may not trip over current circuit breakers but can do enormous damage to bus bars or cables before it becomes a complete short circuit. Utility, industrial, and commercial power systems have additional protection devices to detect relatively small but undesired currents escaping to ground. In residential wiring, electrical regulations may now require Arc-fault circuit interrupters on building wiring circuits, to detect small arcs before they cause damage or a fire.

Symmetric faults can be analyzed via the same methods as any other phenomena in power systems, and in fact many software tools exist to accomplish this type of analysis automatically (see power flow study). However, there is another method which is as accurate and is usually more instructive. First, some simplifying assumptions are made. It is assumed that all electrical generators in the system are in phase, and operating at the nominal voltage of the system. Electric motors can also be considered to be generators, because when a fault occurs, they usually supply rather than draw power. The voltages and currents are then calculated for this base case.

Next, the location of the fault is considered to be supplied with a negative voltage source, equal to the voltage at that location in the base case, while all other sources are set to zero. This method makes use of the principle of superposition.

To obtain a more accurate result, these calculations should be performed separately for three separate time ranges:

- sub transient is first, and is associated with the largest currents
- transient comes between sub transient and steady-state
- steady-state occurs after all the transients have had time to settle
An asymmetric fault breaks the underlying assumptions used in three-phase power, namely that the load is balanced on all three phases. Consequently, it is impossible to directly use tools such as the one-line diagram, where only one phase is considered. However, due to the linearity of power systems, it is usual to consider the resulting voltages and currents as a superposition of symmetrical components, to which three-phase analysis can be applied. In the method of symmetric components, the power system is seen as a superposition of three components:

- a positive-sequence component, in which the phases are in the same order as the original system, i.e., a-b-c
- a negative-sequence component, in which the phases are in the opposite order as the original system, i.e., a-c-b
- a zero-sequence component, which is not truly a three-phase system, but instead all three phases are in phase with each other.

To determine the currents resulting from an asymmetrical fault, one must first know the per-unit zero-, positive-, and negative-sequence impedances of the transmission lines, generators, and transformers involved. Three separate circuits are then constructed using these impedances. The individual circuits are then connected together in a particular arrangement that depends upon the type of fault being studied (this can be found in most power systems textbooks). Once the sequence circuits are properly connected, the network can then be analyzed using classical circuit analysis techniques. The solution results in voltages and currents that exist as symmetrical components; these must be transformed back into phase values by using the A matrix.

Analysis of the prospective short-circuit current is required for selection of protective devices such as fuses and circuit breakers. If a circuit is to be properly protected, the fault current must be high enough to operate the protective device within as short a time as possible; also the protective device must be able to withstand the fault current and extinguish any resulting arcs without itself being destroyed or sustaining the arc for any significant length of time. The magnitude of fault currents differ widely depending on the type of earthing system used, the installation's supply type and earthing system, and its proximity to the supply. For example, for a domestic UK 230 V, 60 A TN-S or USA 120 V/240 V supply, fault currents may be a few thousand amperes. Large low-voltage networks with multiple sources may have fault levels of 300,000 amperes. A high-resistance-grounded system may restrict line to ground fault current to only 5 amperes. Prior to selecting protective devices, prospective fault current must be measured reliably at the origin of the installation and at the furthest point of each circuit, and this information applied properly to the application of the circuits.

2.9 Detecting and locating faults

Overhead power lines are easiest to diagnose since the problem is usually obvious, e.g., a tree has fallen across the line, or a utility pole is broken and the conductors are lying on the ground. Locating faults in a cable system can be done either with the circuit de-energized, or in some cases, with the circuit under power. Fault location techniques can be broadly divided into terminal methods, which use voltages and currents measured at the ends of the cable, and tracer methods, which require inspection along the length of the cable. Terminal methods can be used to locate the general area of the fault, to expedite tracing on a long or buried cable.

In very simple wiring systems, the fault location is often found through inspection of the wires. In complex wiring systems (for example, aircraft wiring) where the wires may be hidden, wiring faults are located with a Time-domain reflect meter. The time domain reflect meter sends a pulse down the wire and then analyzes the returning reflected pulse to identify faults within the electrical wire.

In historic submarine telegraph cables, sensitive galvanometers were used to measure fault currents; by testing at both ends of a faulted cable, the fault location could be isolated to within a few miles, which allowed the cable to be grappled up and repaired. The Murray loop and the Varley loop were two types of connections for locating faults in cables.

Sometimes an insulation fault in a power cable will not show up at lower voltages. A "thumper" test set applies a high-energy, high-voltage pulse to the cable. Fault location is done by listening for the sound of the discharge at the fault. While this test contributes to damage at the cable site, it is practical because the faulted location would have to be re-insulated when found in any case.

In a high resistance grounded distribution system, a feeder may develop a fault to ground but the system continues in operation. The faulted, but energized, feeder can be found with a ring-type current transformer collecting all the phase wires of the circuit; only the circuit containing a fault to ground will show a net unbalanced current. To make the ground fault current easier to detect, the grounding resistor of the system may be switched between two values so that the fault current pulses.

III. DOUBLY-FED INDUCTION GENERATOR

3.1 Introduction
As the penetration of large scale wind turbines into electric power grids continues to increase, electric system operators are placing greater demands on wind turbine power plants. One of the most challenging new interconnection demands for the doubly fed induction generator (DFIG) architecture is its ability to ride through a short-term low or zero voltage event at the point of common coupling (PCC), resulting from a fault on the grid. During extreme voltage sags high per unit currents and shaft torque pulsations occur unless mitigating measures are taken.

Low voltage ride through requirements were first proposed by German electric transmission operators E.ON and VE-T in 2003. In the U.S., FERC order 661A stipulates that the wind turbine must remain connected to the grid and provide fault clearing current in the event that the voltage at the high side of the step up transformer to the transmission system drops to zero volts for a maximum of nine cycles, as the result of a three phase fault. Similar low/zero voltage ride through requirements have evolved in most European countries, each with varying specifications on minimum voltage level and requiring provisions of real or reactive power during fault events. While many grid codes also stipulate ride through of single and two-phase faults, only balanced faults are considered in this paper. In a conventional DFIG wind turbine the machine stator windings are connected to the grid PCC via collection and/or transmission transformers and excited at the grid frequency.

The rotor windings of the DFIG are connected to an ac-converter commonly referred to as the machine side converter (MSC). The ac side of a second dc–ac converter, commonly referred to as the grid side converter (GSC), is connected in parallel with the machine stator windings and PCC. Severe voltage sags and the resulting stator flux response place significant electrical stress on the MSC and mechanical stress on the gearbox. In the stationary frame the stator flux is equal to the integral of the stator voltage minus stator resistive drop. An abrupt stator voltage change produces a constant dc component of stator flux in proportion to the voltage drop.

This dc stator flux component appears as an oscillatory electromagnetic field (EMF) when translated into the synchronous and rotor reference frames. Deep sags and correspondingly large EMF in the rotor reference frame cause the MSC to go into over-modulation, resulting in loss of rotor current regulation. The uncontrolled rotor currents can exceed the semiconductor device ratings and result in damage to the MSC. In addition, this commonly precipitates high transient stator currents and transient torque spikes. Several options have been proposed to improve low voltage ride through. Two modification to the rotor circuit including the addition of either an silicon controlled rectifier (SCR) rotor crowbar circuit or a three phase rectifier and modulated resistive load have demonstrated improvement in the DFIG ride-through capability. As an alternative, brief disconnection of the stator windings during a voltage sag via an SCR static switch has also been shown to reduce torque and current spikes for sags to 15% of nominal.

A modified rotor current control method has been shown to protect the MSC for wind turbine terminal voltage down to about 30% of nominal, with residual torque spikes and oscillations. From an alternate perspective, the authors of first proposed using an inverter connected to the Y point of the DFIG. In series with the stator windings, for the purposes of damping synchronous frame stator flux oscillations. The presence of the converter in series with the stator winding allows a direct handle with which to access the stator flux state variable. The use of a series connected grid side converter was first considered for the purposes of voltage sag ride briefly in, but it properties and limitations were not studied in depth to develop a definitive solution. Further exploration of the series grid side converter DFIG architecture, revealed excellent potential for voltage sag ride through but also short comings in power processing capability a unified DFIG architecture in which the series grid side converter is partnered with a parallel grid side rectifier is presented as an alternative for both DFIG wind turbine power processing and robust voltage sag ride through.

3.2. Doubly-fed electric machine

Doubly-fed electric machines are electric motors or electric generators that have windings on both stationary and rotating parts, where both windings transfer significant power between shaft and electrical system. Doubly-fed machines are useful in applications that require varying speed of the machine's shaft for a fixed power system frequency.

3.3 Classification

Electric machines are either Singly-Fed with one winding set that actively participates in the energy conversion process or Doubly-Fed with two active winding sets. The wound-rotor induction machine and the field-excited synchronous machine are singly-fed machines because only one winding set actively participates in the energy conversion process. Examples of doubly-fed electric machines are the wound-rotor doubly-fed electric machine, the brushless wound-rotor doubly-fed electric machine, and the brushless doubly-fed induction electric machines.

3.4 Features of doubly fed machines
The wound-rotor doubly-fed electric machine is the only electric machine that operates with rated torque to twice synchronous speed for a given frequency of excitation (i.e., 7300 rpm @ 60 Hz and one pole-pair versus 3600 rpm for singly-fed electric machines). Higher speed with a given frequency of excitation gives lower cost, higher efficiency, and higher power density. In concept, any electric machine can be converted to a wound-rotor doubly-fed electric motor or generator by changing the rotor assembly to a multiphase wound rotor assembly of equal stator winding set rating. If the rotor winding set can transfer power to the electrical system, the conversion result is a wound-rotor doubly-fed electric motor or generator with twice the speed and power as the original singly-fed electric machine. The resulting dual-ported transformer circuit topology allows very high torque current without core saturation, all by electronically controlling half or less of the total motor power for full variable speed control.

In practice, the classical wound-rotor doubly-fed "induction" electric motor or generator system has known issues of instability, high maintenance and inefficiency of an integral multiphase slip-ring assembly, and discontinuity about synchronous speed where induction ceases to exist. A practical wound-rotor doubly-fed electric machine system that does not rely exclusively on asynchronous (i.e., induction) principles while symmetrically motoring or generating over its entire speed range has never materialized from the electric machine establishment, despite years of research to find an evolutionary brushless, synchronous, and stable control technology. Consequently, the wound-rotor doubly-fed induction electric machine has been forced into antiquity, except in large installations where efficiency and cost are critical over a limited speed range, such as wind turbines. This may change with recent Brushless Wound-Rotor Doubly-Fed Electric Machine technology development.

3.5 Double fed induction generator

DFIG is an abbreviation for Double Fed Induction Generator, a generating principle widely used in wind turbines. It is based on an induction generator with a multiphase wound rotor and a multiphase slip ring assembly with brushes for access to the rotor windings. It is possible to avoid the multiphase slip ring assembly (see brushless doubly-fed electric machines), but there are problems with efficiency, cost and size. A better alternative is a brushless wound-rotor doubly-fed electric machine.

3.6 Principle of a Double Fed Induction Generator connected to a wind turbine

The principle of the DFIG is that rotor windings are connected to the grid via slip rings and back-to-back voltage source converter that controls both the rotor and the grid currents. Thus rotor frequency can freely differ from the grid frequency (50 or 60 Hz). By using the converter to control the rotor currents, it is possible to adjust the active and reactive power fed to the grid from the stator independently of the generator's turning speed. The control principle used is either the two-axis current vector control or direct torque control (DTC). DTC has turned out to have better stability than current vector control especially when high reactive currents are required from the generator.
and diodes of the converter, a protection circuit (called crowbar) is used.

The crowbar will short-circuit the rotor windings through a small resistance when excessive currents or voltages are detected. In order to be able to continue the operation as quickly as possible an active crowbar has to be used. The active crowbar can remove the rotor short in a controlled way and thus the rotor side converter can be started only after 30-60 ms from the start of the grid disturbance. Thus it is possible to generate reactive current to the grid during the rest of the voltage dip and in this way help the grid to recover from the fault.

A doubly fed induction machine is a wound-rotor doubly-fed electric machine and has several advantages over a conventional induction machine in wind power applications. First, as the rotor circuit is controlled by a power electronics converter, the induction generator is able to both import and export reactive power. This has important consequences for power system stability and allows the machine to support the grid during severe voltage disturbances (low voltage ride through, LVRT). Second, the control of the rotor voltages and currents enables the induction machine to remain synchronized with the grid while the wind turbine speed varies. A variable speed wind turbine utilizes the available wind resource more efficiently than a fixed speed wind turbine, especially during light wind conditions. Third, the cost of the converter is low when compared with other variable speed solutions because only a fraction of the mechanical power, typically 25-30 %, is fed to the grid through the converter, the rest being fed to grid directly from the stator. The efficiency of the DFIG is very good for the same reason.

IV. FUZZY CONTROLLER

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection. To understand why use of fuzzy logic has grown, we must first understand what is meant by fuzzy logic.

Fuzzy logic has two different meanings. In a narrow sense, fuzzy logic is a logical system, which is an extension of multivalve logic. However, in a wider sense fuzzy logic (FL) is almost synonymous with the theory of fuzzy sets, a theory which relates to classes of objects with un sharp boundaries in which membership is a matter of degree. In this perspective, fuzzy logic in its narrow sense is a branch of fl. Even in its more narrow definition, fuzzy logic differs both in concept and substance from traditional multivalve logical systems.

In fuzzy Logic Toolbox software, fuzzy logic should be interpreted as FL, that is, fuzzy logic in its wide sense. The basic ideas underlying FL are explained very clearly and insightfully in Foundations of Fuzzy Logic. What might be added is that the basic concept underlying FL is that of a linguistic variable, that is, a variable whose values are words rather than numbers. In effect, much of FL may be viewed as a methodology for computing with words rather than numbers. Although words are inherently less precise than numbers, their use is closer to human intuition. Furthermore, computing with words exploits the tolerance for imprecision and thereby lowers the cost of solution.

V. SIMULATION AND RESULTS

In order to validate the previous theoretical analysis results, Simulation model with the DFIG is built in the PSCAD/EMTDC software environment. It should be noted that the improved control strategy of the GSC presented in adopted to limit the fluctuation of the dc-link voltage. Besides, the rotate speed is kept constant during grid faults.

The parameters of the 1.5-MW rated DFIG are:

\[ U_{sn} = 690V, f_{n} = 50 \text{ Hz}, L_s = L_r = 2.3192 \text{ p.u.} \]

\[ L_m = 2.1767 \text{ p.u.}, R_i = 0.00756 \text{ p.u.}, R = 0.00533 \text{ p.u.} \]

For the following simulation examples, the output active power of the DFIG is 0.2 p.u. and the grid voltage is 1.0 p.u. before the fault occurs. Additionally, the fault occurs at time \( t = 5.0s \) and results in a symmetrical grid voltage dip down to 0.6 p.u.

Fig. 3 shows the simulation results of the \( d \)-axis and \( q \)-axis components of the stator flux linkage (\( \psi_{sd} \) and \( \psi_{sq} \)), as well as \( e_d \) and \( e_q \).

It can be observed that there are damped fundamental frequency components in the \( d \)-axis and \( q \)-axis components of the stator flux linkage. Meanwhile, the damped fundamental frequency components also exist in \( e_d \) and \( e_q \).

There is no dc component in \( \psi_{sd} \), but there is a dc component whose amplitude is approximately proportional to the depth of grid voltage dip in

![Image](image_url)

Fig.3. \( d \)-axis and \( q \)-axis components of the stator flux linkage, as well as \( e_d \) and \( e_q \) for a voltage dip down to 60%.
Meanwhile, there is an abrupt change in $e_d$ at the moment that the fault occurs, but there is no abrupt change in $e_q$. According to the expressions of $e_d$ and $e_q$ can be rewritten as

\[
\begin{align*}
\psi_{sq} &= \psi_{sq,0} + \psi_{sq,f} = \psi_{sq,0} + \frac{\Delta \psi_{sq}}{L_2}t = \psi_{sq,0} + \frac{\Delta \psi_{sq}}{L_2}t \\
e_d &= \psi_{sd} - e_d = \psi_{sd} - \frac{\Delta \psi_{sd}}{L_1}t = \psi_{sd} - \frac{\Delta \psi_{sd}}{L_1}t
\end{align*}
\]

(1)

As shown in (1), though there is no abrupt change in $\psi_{sd}$ and $\psi_{sq}$, the grid voltage drops suddenly. Hence, there is an abrupt change in $e_d$, but no abrupt change in $e_q$.

**A. Simulation Study under Condition of the Typical First-Order System**

On condition that the inner rotor current controller of the RSC is designed to be a typical first-order system, Fig. 4 shows the comparisons between the simulation results and theoretical analysis results of the $d$-axis and $q$-axis fault components of the rotor current. $\Delta \psi_{sd}$ and $\Delta \psi_{sq}$ represent the simulation results. $\Delta \psi_{sdap}$ and $\Delta \psi_{sqap}$ represent the theoretical analysis results.

Fig. 5 gives the comparisons between the simulation results and theoretical analysis results of the $d$-axis and $q$-axis fault components of the stator current. $\Delta i_{sd}$ and $\Delta i_{sq}$ represent the simulation results. $\Delta i_{sdap}$ and $\Delta i_{sqap}$ represent the theoretical analysis results.

As shown in Figs. 4 and 5, the differences between the simulation results and theoretical analysis results are very small. Notice that there are abrupt changes in $\Delta i_{sdap}$ and $\Delta i_{sdap}$ at the moment that the fault occurs, which are impossible in practice. The reason for this phenomenon is that some lagging elements are neglected for simplification during the theoretical analysis.

**B. Simulation Study under Condition of the Typical Second-Order System**

On condition that the inner rotor current controller of the RSC is designed to be a typical second-order system, Fig. 7 demonstrates the comparisons between the simulation results and theoretical analysis results of the $d$-axis and $q$-axis fault.
components of the rotor current. \( \Delta_{ird} \) and \( \Delta_{irq} \) represent the simulation results. \( \Delta_{irdap} \) and \( \Delta_{irqap} \) represent the theoretical analysis results. It can be obtained that \( \Delta_{ird} \) and \( \Delta_{irq} \) are very small and extremely close to the theoretical analysis results.

Fig. 8 displays the comparisons between the simulation results and theoretical analysis results of the \( d \)-axis and \( q \)-axis fault components of the stator current. \( \Delta_{isd} \) and \( \Delta_{isq} \) represent the simulation results. \( \Delta_{isdap} \) and \( \Delta_{isqap} \) represent the theoretical analysis results. It can be observed that the differences between the simulation results and theoretical analysis results are very small.

Fig. 9 illustrates the simulation result of the stator fault current \( i_{sa} \), the amplitude and phase angle of the fundamental

With Fuzzy logic controller:

Fig. 10. \( d \)-axis and \( q \)-axis fault components of the rotor current for a voltage dip down to 60% under condition of the typical second-order system.

Fig. 11. Stator current for a voltage dip down to 60% under condition of the typical second-order system.
V. CONCLUSION

The PSCAD simulation results verify that the control schemes used in the RSC and GSC increases the fault ride through capability of DFIG as compared to conventional protection schemes and also designed with fuzzy logic controller. The transient characteristics of voltage at faulty condition recovered in a very short time due to adequate supply of reactive power to grid. This ensures better power quality status at the abnormal conditions. Also variation in rotor speed is controlled effectively to ensure stability aspects. The active & reactive power flow is made independent by the decoupling method resulting in better control & performance of DFIG. Hence the operation of hardware protection is not frequent.

VI. REFERENCES


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Improve Quasi-Z-Source Cascade Multilevel Inverter-Based Grid-Tie Single-Phase Photovoltaic System Using Fuzzy Logic

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Abstract: An effective control method, including system-level control and pulse width modulation for quasi-Z-source cascade multilevel inverter (qZS-CMI) based grid-tie photovoltaic (PV) power system is proposed. The system-level control achieves the grid-tie current injection, independent maximum power point tracking (MPPT) for separate PV panels, and dc-link voltage balance for all quasi-Z-source H-bridge inverter (qZS-HBI) modules. The complete design process is disclosed. A multilevel space vector modulation (SVM) for the single-phase qZS-CMI is proposed to fulfill the synthetization of the step-like voltage waveforms. Simulation and experiment based on a seven-level prototype are carried out to validate the proposed methods. Here we propose fuzzy logic controller for better result compared to previous one.

I. INTRODUCTION

A recent upsurge in the study of photovoltaic (PV) power generation emerges, since they directly convert the solar radiation into electric power without hampering the environment. However, the stochastic fluctuation of solar power is inconsistent with the desired stable power injected to the grid, owing to variations of solar irradiation and temperature. To fully exploit the solar energy, extracting the PV panels’ maximum power and feeding them into grids at unity power factor become the most important. The contributions have been made by the cascade multilevel inverter (CMI) [1], [2]. Nevertheless, the H-bridge inverter (HBI) module lacks boost function so that the inverter KVA rating requirement has to be increased twice with a PV voltage range of 1:2; and the different PV panel output voltages result in imbalanced dc-link voltages.

The extra dc–dc boost converters were coupled to PV panel and HBI of the CMI to implement separate maximum power point tracking (MPPT) and dc-link voltage balance [3], [4]. However, each HBI module is a two-stage inverter, and many extra dc–dc converters not only increase the complexity of the power circuit and control and the system cost, but also decrease the efficiency. Recently, the Z-source/quasi-Z-source cascade multilevel inverter (ZS/qZS-CMI)-based PV systems were proposed in [5]–[8]. They possess the advantages of both traditional CMI and Z-source topologies. For example, the ZS/qZS-CMI:

The main contributions of this paper include:
1) A novel multilevel space vector modulation (SVM) technique for the singlephase qZS-CMI is proposed, which is implemented without additional resources;
2) A grid-connected control for the qZS-CMI based PV system is proposed, where the all PV panel voltage references from their independent MPPTs are used to control the grid-tie current; the dual-loop dc-link peak voltage control is employed in every qZS-HBI module to balance the dc-link voltages;

3) The design process of regulators is completely presented to achieve fast response and good stability; and 4) simulation and experimental results verify the proposed PWM algorithm and control scheme.

II. MULTILEVEL INVERTER

In response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter [1]–[3].

As reported in the literature, the H-bridge cascade inverter has been used in several practical instances for broadcasting amplifier [4], plasma [5], industrial drive [6] as well as STATCOM [7] applications etc. The main limitation of the H-bridge cascade inverter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. For STATCOM application, where the isolated supplies are not required, the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates over-sizing of the dc link capacitors.

III. SPACE VECTOR MODULATION

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM). It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

3.1 Principle

Fig 3.1 Topology of a basic three phase inverter.

A three-phase inverter as shown to the right converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg, i.e. if A+ is on then A− is off and vice versa. This leads to eight possible switching vectors for the inverter, V₀ through V₇ with six active switching vectors and two zero vectors.
IV. Fuzzy Controller

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection. To understand why use of fuzzy logic has grown, we must first understand what is meant by fuzzy logic. Fuzzy logic has two different meanings. In a narrow sense, fuzzy logic is a logical system, which is an extension of multivalve logic. However, in a wider sense fuzzy logic (FL) is almost synonymous with the theory of fuzzy sets, a theory which relates to classes of objects with un sharp boundaries in which membership is a matter of degree. In this perspective, fuzzy logic in its narrow sense is a branch of fl. Even in its more narrow definition, fuzzy logic differs both in concept and substance from traditional multivalve logical systems.

In fuzzy Logic Toolbox software, fuzzy logic should be interpreted as FL, that is, fuzzy logic in its wide sense. The basic ideas underlying FL are explained very clearly and insightfully in Foundations of Fuzzy Logic. What might be added is that the basic concept underlying FL is that of a linguistic variable, that is, a variable whose values are words rather than numbers. In effect, much of FL may be viewed as a methodology for computing with words rather than numbers. Although words are inherently less precise than numbers, their use is closer to human intuition. Furthermore, computing with words exploits the tolerance for imprecision and thereby lowers the cost of solution.

V. Description of QZS-CMI-Based Grid-Tie PV Power System

Fig. 5.1 shows the discussed qZS-CMI-based grid-tie PV power system. The total output voltage of the inverter is a series summation of qZS-HBI cell voltages. Each cell is fed by an independent PV panel. The individual PV power source is an array composed of identical PV panels in parallel and series. A typical PV model in [12] is performed by considering both the solar irradiation and the PV panel temperature.

5.1 qZS-CMI

The qZS-CMI combines the qZS network into each HBI module. When the th qZS-HBI is in nonshoot-through states, it will work as a traditional HBI. There are

\[ \hat{v}_{DCk} = \frac{1}{1 - 2D_k} v_{PVk} = B_k v_{PVk}, \quad v_{Hk} = S_k \hat{v}_{DCk} \]

while in shoot-through states, the qZS-HBI module does not contribute voltage. There are

\[ \hat{v}_{DCk} = 0, \quad v_{Hk} = 0. \]

For the qZS-CMI, the synthesized voltage is

\[ v_H = \sum_{k=1}^{n} v_{Hk} = \sum_{k=1}^{n} S_k \hat{v}_{DCk} \]

where is the output voltage of the th PV array; is the dc-link voltage of the th qZS-HBI module; and represent the shoot-through duty ratio and boost factor of the th qZS-HBI, respectively, is the output voltage of the th module, and is the switching function of the th qZS-HBI.
5.2 Control Strategy

The control objectives of the qZS-CMI based grid-tie PV system are:

1) The distributed MPPT to ensure the maximum power extraction from each PV array;
2) The power injection to the grid at unity power factor with low harmonic distortion;
3) The same dc-link peak voltage for all qZS-HBI modules.

The overall control scheme of Fig. 5.1 is proposed to fulfill these purposes. For achieving the first two goals, the closed loops are employed, as Fig. 5.1(a) shows.

1) Total PV array voltage loop adjusts the sum of PV array voltages tracking the sum of PV array voltage references by using a proportional and integral (PI) regulator. Each PV array voltage reference is from its MPPT control independently.

2) Grid-tie current loop ensures a sinusoidal grid-injected current in phase with the grid voltage. The total PV array voltage loop outputs the desired amplitude of grid-injected current. A Proportional + Resonant (PR) regulator enforces the actual grid current to track the desired grid-injected reference. The current loop output’s total modulation signal subtracts the modulation signal sum of the second, third, , and th qZS-HBI modules to get the first qZS-HBI module’s modulation signal.

3) The separate PV array voltage loops regulate the other PV array voltages to achieve their own MPPTs through the PI regulators, such as to , respectively. With the total PV array voltage loop control, the PV arrays fulfill the distributed MPPT. In addition, the voltage feed forward control is used to generate each qZS-HBI module’s modulation signal, which will reduce the regulators’ burden, achieve the fast dynamic response, and minimize the grid voltage’s impact on the grid-tie current. For the third goal, the dc-link peak voltage is adjusted in terms of its shoot-through duty ratio for each qZS-HBI module, as Fig. 1(b) shows. A proportional ( ) regulator is employed in the inductor current loop to improve the dynamic response, and a PI regulator of the dc-link voltage loop ensures the dc-link peak voltage tracking the reference. Finally, the independent modulation signals and shoot through duty ratios of the qZS-CMI, , are combined into the proposed multilevel SVM to achieve the desired purposes.

5.3 System Modeling and Control

Fig. 5.2 shows block diagram of the proposed grid-tie control with the system model for the qZS-CMI based PV power system. The details will be explained as follows.

5.3.1 Grid-Tie Current Loop

The th qZS-HBI module has following dynamic:

\[ i_{L_{k}} = i_{P_{k}} + C_{P} \frac{dV_{P_{k}}}{dt} \]

where is the current of qZS inductor , is the th PV array’s current, and is the capacitance of PV array terminal capacitor. The qZS-CMI based grid-tie PV system has

\[ v_{H} = v_{g} + L \frac{d\dot{i}_{s}}{dt} + r \dot{i}_{s} \]

where is the grid voltage, is the grid-injected current, is the filter inductance, and is its parasitic resistance. The transfer function of the grid-injected current can be
\( v_{mk} = v'_{mk} + V_g(s) G_{vfk}(s) \)

With

\( G_{vfk}(s) = \frac{1}{n G_{invk}(s)} \)

\( G_{invk}(s) = \frac{V_{Hk}(s)}{V_{mk}(s)} = \hat{v}_{DCk} \)

where is the regulated modulation signal from the separate voltage control of the th module, as Fig. 5.2 shows.

From (8) and (9), we have

\[
V_{Hf}(s) = \sum_{k=1}^{n} v_{mk} G_{invk}(s)
\]

\[
= \sum_{k=1}^{n} [v'_{mk} G_{invk}(s) + V_{g}(s) G_{vfk}(s) G_{invk}(s)].
\]

At the dc-link peak voltage control, all dc-link peak voltages are the same. The qZS-HBI modules have the same transfer function, and we assume

\( G_{invk}(s) = G_{inv}(s), \quad k \in \{1, 2, \ldots, n\}. \)

Using (6)–(11), the grid-injected current will be

\[
I(s) = G_f(s) G_{inv}(s) \sum_{k=1}^{n} v'_{mk}.
\]

Then, the current loop of Fig. 5.2 is simplified to Fig. 5.3, and the open-loop transfer function can be obtained as

\[
G_{io}(s) = \frac{I_o(s)}{V_{m}(s)} = G_{inv}(s) G_f(s) = \frac{\hat{v}_{DCk}}{L_f s^3 + r_f}.
\]

With the compensation of the PR regulator, the transfer function Becomes

\[
G_{icom}(s) = G_{PRi}(s) G_{io}(s)
\]

\[
= \frac{\hat{v}_{DCk} (k_i P s^2 + k_i R \omega_0^2)}{L_f s^3 + r_f s^2 + L_f \omega_0^2 s + r_f \omega_0^2}.
\]

Fig. 5.3. Simplified block diagram of the grid-current closed loop.
Consequently, the closed-loop transfer function of grid-tie current control can be obtained in (15), shown at the bottom of the page.

### 5.3.2 PV Voltage Loop

From (5), we have

\[ V_{PVk}(s) = \frac{1}{C_p s} \left[ I_{PVk}(s) - I_{L1k}(s) \right] \]

In addition, the output power of each qZS-HBI module equals to its input power in the non-shoot-through state, the th qZS-HBI module has the power equation

\[ \frac{1}{2} \hat{\bar{V}}^2 H_k \tilde{L}_1 = \bar{V} D CK \tilde{L}_1 = V PV_k \tilde{b} L1_{k-ns h} \]

Where is the average current of inductor in nonshoot-through state. Using (1), can be solved as

\[ \tilde{b} L1_{k-ns h} = \tilde{V} PV_k = \tilde{b} PV_k. \]

Combining (18) and (19), the average current of inductor is

\[ \bar{V} L1_{k} = D_k \tilde{b} L1_{k-ns h} + (1 - D_k) \tilde{b} L1_{k-ns h} + \hat{\bar{b}} (1 - D_k) \bar{V} R \]

Then, the block diagrams of total and separate PV voltage loops can be obtained in Figs. 5 and 5.5

If is considered as disturbance, with (20) and Fig. 5.5, the transfer function of the total PV array voltage loop is given by (21), shown at the bottom of the page, where the coefficients and are

\[ h_1 = \sum_{k=1}^{n} \frac{(1 - D_k) G_{Fe} (s)}{\bar{V} DC (1 - 2D_k)} \]

\[ h_2 = \tilde{\bar{V}} DC k_1 R \omega_0 + \tilde{\bar{V}} DC k_2 R \omega_0 + r_f \omega_0^2. \]

The PI regulator is applied to track the total reference voltage coming from MPPT algorithm. Thus, the open-loop transfer function of total PV voltage loop after compensation can be obtained by

\[ G_{total}(s) = G_{PI}(s)G_{vol}(s) = \frac{Num_{total}(s)}{Den_{total}(s)} \]

Where
\[\text{Num}_{\text{com}}(s) = h_1 k_p k_{f} s^3 + h_1 k_p k_{i} s^2 + h_1 k_p (k_{i} \omega_0 + k_{i} R) s + k_{i} R \omega_0\]

\[\text{Den}_{\text{com}}(s) = 2C_p L_f s^5 + 2C_p (f_f + k_p \hat{v}_{DCB}) s^4 + 2C_p L_f \omega_0^2 s^3 + 2C_p \hat{h}_2 s^2.\]

Fig. 5.6. Block diagram of the \(m\) module’s dc-link peak voltage control. The closed-loop transfer function is

\[G_{vct}(s) = \frac{V_{PV}(s)}{V_{PV}(s)} = \frac{-G_{vcom}(s)}{1 - G_{vcom}(s)}\]

Similarly, from Fig. 5.5, the transfer function of the \(m\) qZS-HBI module’s PV voltage loop, \(v_m\), is

\[G_{vom}(s) = \frac{V_{PVm}(s)}{V_{PVm}(s)} = \frac{-G_{vcom}(s)}{1 - G_{vcom}(s)}\]

which is compensated by PI regulator. Then, the resultant open-loop transfer function of the \(m\) qZS-HBI module’s PV voltage loop becomes

\[G_{vom}(s) = G_{vom}(s)G_{lom}(s) = \frac{-i_m(s)}{1 - G_{vom}(s)}\]

Also, the closed-loop transfer function is obtained as

\[G_{vom}(s) = \frac{V_{PVm}(s)}{V_{PVm}(s)} = \frac{-G_{vom}(s)}{1 - G_{vom}(s)}.\]

5.3.3 DC-Link Voltage Control

The independent dc-link peak voltage control based on the inductor-current and the capacitor-voltage is performed for each qZS-HBI module, as Fig. 5.1(b) shows. From [15], the \(m\) qZS-HBI module’s transfer functions from the shoot-through duty ratio to the dc-link peak voltage, \(d_m\), and from the shoot-through duty ratio to the inductor-current, \(i_m\), can be obtained, respectively.

With the employed proportional regulator at the coefficient for the inductor current loop, as the block diagram of Fig. 5.6 shows, the closed-loop transfer function of inductor current can be obtained by

\[G_{idc}(s) = \frac{d_k(s)}{I_{L2k}(s)} = \frac{K_{ATk}}{1 + K_{ATk}G_{idc}(s)}\]

A PI regulator with the transfer function of is cascaded to the inductor current loop for controlling the dc-link peak voltage, as shown in Fig. 5.6. Therefore, the \(m\) qZS-HBI module’s dc-link peak voltage control has the open-loop transfer function

\[G_{Vdc}(s) = G_{viP}\frac{s}{G_{iDc}(s)}\]

Fig. 5.7. Proposed multilevel SVM for the single-phase qZS-CMI. (a) Switching pattern of one qZS-HBI module. (b) Synthetization of voltage vectors for the qZS-CMI. and the closed-loop transfer function

\[G_{Vdc}(s) = \frac{d_k(s)}{V_{DC}(s)} = \frac{G_{viP}\frac{s}{G_{iDc}(s)}}{1 + G_{viP}\frac{s}{G_{iDc}(s)}G_{Vdc}(s)}\]
5.5 Proposed Multilevel SVM for QZS-CMI

As the qZS network is embedded to the HBI module, the SVM for each qZS-HBI can be achieved by modifying the SVM technique for the traditional single-phase inverter [15]. Using the first qZS-HBI module of Fig. 5.1 as an example, the voltage vector reference is created through the two vectors and, by

\[ U_{\text{ref}1} = U_1 \frac{T_1}{T_s} + U_0 \frac{T_0}{T_s} \]

where and is the carrier frequency; the time interval is the duration of active vectors, and is the duration of traditional zero voltage space vectors. Thus, the switching times for the left and right bridge legs in traditional HBI are. However, the shoot-through states are required for the independent qZS-HBI module. For this purpose, a delay of the switching times for upper switches or a lead of the switching times for lower switches are employed at the transition moments, as Fig. 5.7(a) shows. During each control cycle, the total time of shoot-through zero state is equally divided into four parts. The time intervals of and remain unchanged; and are the modified times to generate the shoot-through states; and are the switching control signals for the upper switches, and are that for the lower switches, .

In this way, the shoot-through states are distributed into the qZS-HBI module without additional switching actions, losses, and resources. To generate the step-like ac output voltage waveform from the qZS-CMI, a phase difference, in which is the number of reference voltage vectors in each cycle, is employed between any two adjacent voltage vectors, as Fig. 5.7(b) shows. The total voltage vector is composed of reference vectors from the qZS-HBI modules.

VI. Simulation And Experimental Verifications

A seven-level qZS-CMI for grid-connected PV power system is prototyped. Two Agilent E5360A Solar Array Simulators (SAS) are used to emulate the electrical behavior of PV arrays. Each SAS has two channel outputs, and each channel is with maximum 120-V maximum power point (MPP) voltage ( ) and 5-A MPP current ( ). Simulation and experimental results are shown in Figs. 6.1–6.5.

![Fig. 6.1. Simulation results of qZS-CMI at different PV array voltages.](image)

6.1 DC-Link Voltage Balance Test

The different PV array voltages are performed for the three qZS-HBI modules. The second module’s PV voltage is set to 60 V and the others are at 90 V. A 50- resistor is used as ac load in this test. All of the voltages in experimental results are 100 V/div. From (1), the 136-V dc-link voltage of qZS-HBI module is required to support the 230-V grid. Fig. 6.1 shows the simulation results, where the second module’s dc-link peak voltage is boosted to the same voltage value when compared with other modules, but with a longer shoot-
through time interval. Also, the qZS-CMI outputs the seven-level voltage with equal voltage step from one level to another level. Fig. 6.2 shows the experimental results. We can find that the same qZS-CMI output voltages and currents are achieved in Fig. 6.2 (or Fig. 6.2), which is derived from the designed dc-link peak voltage control.

6.2 Grid-Tie Investigation

The qZS-CMI is connected to the grid in order to test the proposed grid-tie control. Fig. 6.3 shows the PV array’s power voltage characteristics. The measured PV array voltage and current of each module are used to calculate the actual PV power and the MPPT algorithm searches for the PV voltage reference at the MPP, which is refreshed every 0.05 s. Here, the perturbation and observation (P&O)MPPT strategy is applied in considering the excellent tracking efficiency and easy implementation [16]. At first, the three modules are all working at 900 W/m, and all of the initial voltage references of MPPT algorithms are given at 105 V from Fig. 6.3. The second module’s irradiation decreases to 600 W/m from 1 to 2 s in simulation. Fig. 6.5 shows the simulation results. In the experiments, the same test conditions of irradiation and temperature can be implemented by setting the curves of Agilent SAS. Fig. 6.5 shows the experimental results. Fig. 6.5(a) shows the total PV voltage (sum of three PV panel voltages) and reference, PV panel voltages and references of modules 2 and 3, respectively. Fig. 6.5(b) is the enlarged detail of Fig. 6.5(a). It can be seen that the excellent tracking performance is achieved during 0–1 s;

Fig. 6.2. Experimental results of qZS-CMI at different PV array voltages. (a) Two modules’ PV array voltages and dc-link voltages. (b) Two PV array voltages, seven-level output voltage, and load current.

Fig. 6.3. PV array power–voltage characteristic. Even though the second module’s PV irradiation changes after 1 s, the still tracks the reference very well after a very short transient.

Fig. 6.5(c) and (d) shows that the grid-injected current is exactly in phase with the grid voltage even at the irradiation changing moment. The solar irradiation does not affect the seven-level staircase output voltage of qZS-CMI, but the lower irradiation makes the grid-injected current reduced. The identical experimental results are shown in Fig. 6.5. As in Fig. 6.5(a), the lower solar irradiation reduces the second
6.5. Simulation results at the grid-tie case. (a), (b) For PV voltages at MPPT. (c), (d) For qZS-CMI output voltage, grid voltage, and current. module’s PV panel current, the first and third modules’ PV panel currents are not changed due to their constant irradiations.

Fig. 6.6. Experimental results at the grid-tie case. (a) Three PV panel currents. (b) Second module’s PV panel voltage, qZS-CMI output voltage, grid voltage, and the grid-injected current. (c) Results zoomed in when the second module’s PV irradiation changes from 900 to 600 W/m .

The second module’s low irradiation causes the system power reduced, so the grid-injected current decreases, as Fig. 6.5(c) shows. No matter the solar irradiation changes or not, the qZS-CMI always outputs consistent voltage, which verifies the voltage balance ability. In simulation and experiments, the irradiation change may be derived from the shading of cloud or other objects. Figs. 6.5 and 6.5 validate the proposed control methods.

With fuzzy logic controller:
panel currents are not changed due to their constant irradiations.

Conclusion

This paper proposed a control method for qZS-CMI based single-phase grid-tie PV system. The grid-injected power was fulfilled at unity power factor, all qZS-HBI modules separately achieved their own maximum power points tracking even if some modules’ PV panels had different conditions. Moreover, the independent dc-link voltage closed-loop control ensured all qZS-HBI modules have the balanced voltage, which provided the high quality output voltage waveform to the grid. The control parameters were well designed to ensure system stability and fast response. A multilevel SVM integrating with shoot through states was proposed to synthesize the staircase voltage waveform of the single-phase qZS-CMI.

The simulation and experiment were carried out on the seven-level qZS-CMI prototype. The qZS-CMI based grid-tie PV system was tested. The simulation and experimental results verified the proposed qZS-CMI based grid-tie PV power system and the proposed control method. In principle, the proposed system can work with the weak grid, even though this paper did not address this topic. In future work, we will focus on the application to the weak grid, and the detailed analysis and experimental results will be disclosed in the next paper.

References


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Photovoltaic Power Generation System with Five Level Inverter

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Abstract—In this paper, Photovoltaic Power Generation System with Five Level Inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss, harmonic distortion, and electromagnetic interference caused by the switching operation of power electronic devices. Two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the five-level inverter. The input of the dual-buck converter is two dc capacitor voltage sources. The dual-buck converter converts two dc capacitor voltage sources to a dc output voltage with three levels and balances these two dc capacitor voltages. The output voltage of the dual-buck converter supplies to the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a five-level ac voltage. The output current of the five-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid. Simulation prototype is developed to verify the performance of the developed renewable power generation system. Simulation results show that the developed renewable power generation system reaches the expected performance.

I. Introduction

THE conventional single-phase inverter topologies for gridconnection include half-bridge and full bridge. The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and uni polar modulation. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is
proportional to the switching frequency, voltage jump of each switching, and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced. Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. The conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types as shown in Fig. 1. Fig. 1(a) shows the basic configuration of a diode-clamped multilevel inverter. As can be seen, it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The voltage difference of each level is \( \frac{V_{dc}}{2} \) (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter, the voltages of these two dc capacitors must be controlled to be equal. The control for balancing these two dc capacitors is very important in controlling the diode-clamped multilevel inverter, and it is very hard under the light load. If the five-level output voltage is expected, extra two diodes and four power electronic switches are required Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four power electronic switches. The voltage on each dc capacitor is controlled to be \( \frac{V_{dc}}{2} \), and the output voltage of the basic flying capacitor multilevel inverter has three levels. The voltage difference of each level is also \( \frac{V_{dc}}{2} \) (the voltage on a dc capacitor).

Fig. 1 shows the circuit configuration of the basic cascade H-bridge multilevel inverter [8]. As can be seen, it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is \( \frac{V_{dc}}{2} \), and the output voltage of each full-bridge inverter can be controlled to be \( \frac{V_{dc}}{2} \), 0, and \( -\frac{V_{dc}}{2} \). Thus, the voltage levels of the output voltage of the cascade full-bridge multilevel inverter are \( V_{dc} \), \( \frac{V_{dc}}{2} \), 0, \( -\frac{V_{dc}}{2} \), and \( -V_{dc} \). This topology has advantages of fewer components being required compared with other multilevel inverters under the output voltage with the same levels, and its hardware circuit can be modularized because the configuration of each full bridge is the same capacitor.

Fig. 1. Circuit configuration of conventional single-phase multilevel inverter.
II. Photovoltaic

Photovoltaic (PV devices) or “solar cells” – change sunlight directly into electricity. The photovoltaic cell was discovered in 1954 by Bell Telephone researchers examining the sensitivity of a properly prepared silicon wafer to sunlight. Beginning in the late 1950s, photovoltaic cells were used to power U.S. space satellites. The success of PV in space generated commercial applications for this technology. The simplest photovoltaic systems power many of the small calculators and wrist watches used everyday. More complicated systems provide electricity to pump water, power communications equipment, and even provide electricity to our homes.

Solar Power Plants

indirectly generate electricity when the heat from solar thermal collectors is used to heat a fluid which produces steam that is used to power generator. Out of the 15 known solar electric generating units operating in the United States at the end of 2006, 10 of these are in California, and 5 in Arizona. No statistics are being collected on solar plants that produce less than 1 megawatt of electricity, so there may be smaller solar plants in a number of other states.

III. Circuit Configuration

Fig. 2 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system. As can be seen, it is configured by a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches SW1 and SW2. The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the five-level inverter. The dc–dc converter is a boost converter, and it performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This five-level inverter is configured by two dc capacitors, a dualbuck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The two dc capacitors perform as energy buffers between the dc–dc
converter and the five-level inverter. The output of the dual-buck converter is connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the full-bridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual-buck converter.

IV. Operation Principle Of Five-Level Inverter

The operation of this five-level inverter can be divided into eight modes. Modes 1–4 are for the positive half-cycle, and modes 5–8 are for the negative half-cycle. Fig. 3 shows the operation modes of five-level inverter. As can be seen, the power electronic switches of the full-bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the dc power into ac power for commutating. As seen in Fig. 3(a)–(d), the power electronic switches S4 and S7 are in the ON state, and the power electronic switches S5 and S6 are in the OFF state during the positive half-cycle. On the contrary, the power electronic switches S4 and S7 are in the OFF state, and the power electronic switches S5 and S6 are in the ON state during the negative half-cycle. Since the dc capacitor voltages VC2 and VC3 are balanced by controlling the five-level inverter, the dc capacitors VC2 and VC3 can be represented as follows:

\[ V_{C2} = V_{C3} = \frac{1}{2} V_{dc}. \]  

(1)

The operation modes of this five-level inverter are stated as follows.

Mode 1: Fig. 3(a) shows the operation circuit of mode 1. The power electronic switch of the dual-buck converter S2 is turned ON and S3 is turned OFF. DC capacitor C2 is discharged through S2, S4, the filter inductor, the utility, S7, and D3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc/2. Mode 2: Fig. 3(b) shows the operation circuit of mode 2. The power electronic switch of the dual-buck converter S2 is turned OFF and S3 is turned ON. DC capacitor C3 is discharged through D2, S4, the filter inductor, the utility, S7, and S3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc/2. Mode 3: Fig. 3(c) shows the operation circuit of mode 3. Both power electronic switches S2 and S3 of the dual-buck converter are turned OFF. The current of the filter inductor flows through the utility, S7, D3, D2, and S4. Both output voltages of the dual-buck converter and five-level inverter are 0. Mode 4: Fig. 3(d) shows the operation circuit of mode 4. Both power electronic switches S2 and S3 of the dual-buck converter are turned ON. DC capacitors C2 and C3 are discharged together through S2, S4, the filter inductor, the utility, S7, and S3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc. Modes 5–8 are the operation modes for the negative half-cycle. The operations of the dual-buck converter under modes 5–8 are similar to that under modes 1–4, and the dual-buck converter can also generate three voltage levels Vdc/2, Vdc/2, 0, and Vdc, respectively. However, the operation of the full-bridge inverter is the opposite. The power electronic switches S4 and S7 are in the OFF state, and the power electronic switches S5 and S6 are in the ON state during the negative half-cycle. Therefore,
The output voltage of the five-level inverter for modes 5–8 will be \(-\frac{V_{dc}}{2}, -\frac{V_{dc}}{2}, 0,\) and \(-V_{dc}\), respectively. Considering operation modes 1–8, the full-bridge inverter converts the dc output voltage of the dual-buck converter with three levels to an ac output voltage with five levels which are \(V_{dc}, \frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2},\) and \(-V_{dc}\). The operation of power electronic switches S2 and S3 should guarantee the output voltage of the dual-buck converter is higher than the absolute of the utility voltage. The waveforms of output voltage of five-level inverter and utility voltage are shown in Fig. 4. Due to the operation of full-bridge inverter, the voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the five-level inverter. When the absolute of the utility voltage is smaller than \(\frac{V_{dc}}{2}\), the output voltage of the dual-buck converter should change between \(V_{dc}/2\) and 0. Accordingly, the power electronics of five-level inverter is switched between modes 1 or 2, and mode 3 during the positive half-cycle. On the contrary, the power electronics of five-level inverter is switched between modes 5 or 6, and mode 7 during the negative half-cycle. One of the power electronic switches S2 and S3 is in the OFF state and the other is switched in high frequency during one PWM period. Fig. 5(a) shows the equivalent circuit for the dc side of the five-level inverter under \(|v_s| < \frac{V_{dc}}{2}\). As seen in Fig. 5(a), the equivalent circuit is a conventional buck converter. DC voltage source \(V_{cx}\) may be dc capacitor voltage \(V_{C2}\) or \(V_{C3}\), and it depends on which power electronic switch S2 or S3 is switching in high frequency. As the power electronic switch is turned ON, the change rate of the output current can be represented as follows:

\[
\frac{d|i_o|}{dt} = \frac{V_{C,x} - |v_s|}{L}
\]  

(2)

where \(L\) is the inductance of the filter inductor. The change rate of the output current is positive. Thus, the output current \(|i_o|\) increases when the power electronic switch is turned ON. As the power electronic switch is turned OFF, the change rate of the output current can be represented as follows:

\[
\frac{d|i_o|}{dt} = -\frac{|v_s|}{L}.
\]  

(3)

The change rate of the output current is negative, meaning the output current \(|i_o|\) will decrease when the power electronic switch is turned OFF. As seen in (2) and (3), the output current \(|i_o|\) can be controlled by controlling the ON/OFF operation of the power electronic switch to track a reference current signal. When the absolute of the utility voltage is higher than \(V_{dc}/2\), the output voltage of the dual-buck converter should be changed between \(V_{dc}\) and \(V_{dc}/2\). Accordingly, the five-level inverter is operated in mode 4, and 1 or 2 during the positive half-cycle, and it is switched in mode 8, and 5 or 6 during the negative half-cycle. One of power electronic switches S2 and S3 is still turned ON and the other is switched in high frequency during one PWM period. Fig. 5(b) shows the equivalent circuit for the dc side of the five-level inverter.
inverter under $|v_s| > V_{dc}/2$. The dc voltage source $V_{dc}$ is the summation of dc capacitor voltages $V_{C2}$ and $V_{C3}$. As seen in Fig. 5(b), it differs from the conventional buck converter, where voltage source $V_{Cx}$ is connected to the diode in series. Voltage source $V_{Cx}$ may be dc capacitor voltage $V_{C2}$ or $V_{C3}$, and it depends on which power electronic switch $S3$ or $S2$ is switching in high frequency.

Fig. 2. Circuit configuration of the developed photovoltaic power generation system.

Fig. 3. Operation modes of the five-level inverter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

Fig. 4. Waveforms of output voltage and utility voltage.

Fig. 5. Equivalent circuit. (a) $|v_s| < V_{dc}/2$. (b) $|v_s| > V_{dc}/2$.

V. Voltage Balance Of Five-Level Inverter

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages $V_{C2}$ and $V_{C3}$ can be controlled by the power electronic switches $S2$ and $S3$ easily. When the absolute of the utility voltage is smaller than $V_{dc}/2$, one power electronic switch either $S2$ or $S3$ is switched in high frequency and the other is still in the OF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages $V_{C2}$ and $V_{C3}$. If dc capacitor voltage $V_{C2}$ is higher than dc capacitor voltage $V_{C3}$, power electronic switch $S2$ is switched in high frequency. In
In this situation, the voltage source VCx in Fig. 5(a) is VC2, and C2 will be discharged. Thus, the dc capacitor voltages VC2 decreases and VC3 does not change. On the contrary, power electronic switch S3 is switched in high frequency when voltage VC3 is higher than voltage VC2. In this situation, the voltage source VCx in Fig. 5(a) is VC3. Thus, the dc capacitor voltages VC3 decreases and VC2 does not change. In this way, the voltage balance of C2 and C3 can be achieved. When the absolute of the utility voltage is higher than Vdc/2, one power electronic switch either S2 or S3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages VC2 and VC3. If dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, the power electronic switch S3 is switched in high frequency. The voltage source VCx in Fig. 5(b) is dc capacitor voltage VC2. When the power electronic switch S3 is turned ON, both C2 and C3 are discharged. However, only C2 supplies the power when the power electronic switch S3 is turned OFF. Thus, C3 will discharge more power than that of C2. In this way, the voltage balance of C2 and C3 can be achieved. As mentioned earlier, the operation of power electronic switches S2 and S3 can be summarized as Table I. The voltages of capacitors C2 and C3 can be easily balanced compared with the conventional multilevel inverter.

<table>
<thead>
<tr>
<th>VCx&gt;Vdc/2</th>
<th>VCx&lt;Vdc/2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1: PWM</td>
<td>S1: PWM</td>
</tr>
<tr>
<td>S0: on</td>
<td>S0: off</td>
</tr>
<tr>
<td>S2: off</td>
<td>S2: PWM</td>
</tr>
<tr>
<td>S3: on</td>
<td>S3: on</td>
</tr>
</tbody>
</table>

VI. Control Block Diagram

The developed photovoltaic power generation system consists of a dc–dc power converter and the five-level inverter. The five-level inverter performs the functions of converting the dc power into high-quality ac power and injecting it into the utility, balancing two dc capacitor voltages VC2 and VC3, and detecting the islanding operation. The dc–dc converter boosts the output voltage of the solar cell array and performs the MPPT to extract the maximum output power of the solar cell array. The controllers of both the dc–dc converter and the five-level inverter are explained as follows.

A. Five-Level Inverter

Fig. 6 shows the control block diagram of five-level inverter. In the operation of the
five-level inverter, the dc bus voltage must be regulated to be larger than the peak voltage of the utility, and the dc capacitor voltages of C2 and C3 must be controlled to be equal. Besides, the five-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. As seen in Fig. 6, the voltages of dc capacitors C2 and C3 are detected and then added to obtain a dc bus voltage Vdc. The added result is subtracted from a dc bus setting voltage Vdcset. The dc bus setting voltage Vdcset is larger than the peak voltage of the utility. The subtracted result is sent to a P-I controller. An islanding detection is also incorporated into the control of the five-level inverter. The concept of this islanding detection was proposed by authors [23]. However, it will not be addressed in this paper.

As seen in Fig. 6, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. If the RMS value of the utility current is smaller than the low threshold value, the output of the hysteresis comparator is high, meaning the condition of islanding operation or power balance occurs. On the contrary, the output of the hysteresis comparator is low when the RMS value of the utility current is larger than the high threshold value, meaning the utility is normal. The output of the hysteresis comparator is sent to a signal generator. The output signal of the signal generator is an islanding control signal Sa. The islanding control signal is a dc signal with unity amplitude if the output of the hysteresis comparator is low. On the contrary, the islanding control signal is a square wave with a frequency of 20 Hz (disturbance signal for islanding detection) when the output of the hysteresis comparator is high. The outputs of the PI controller and signal generator are sent to a multiplier, and the product of the multiplier is the amplitude of the reference signal. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate an unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The product of this multiplier is the reference signal of the output current for the five-level inverter. The output current of the five-level inverter is detected by a current sensor. The reference signal and detected signal for the output current of the five-level inverter are sent to a subtractor. The subtracted result is sent to a current-mode controller. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. The detected dc capacitor voltages VC2 and VC3 are also sent to a comparator to obtain signal Sb. When dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, Sb is a high value. On the contrary, Sb is a low value when dc capacitor voltage VC2 is smaller than dc capacitor voltage VC3. DC voltage Vdc is also sent to an amplifier with
a gain of 0.5 to obtain voltage signal Vdc/2. The detected utility voltage is sent to an absolute circuit to obtain voltage signal |vs |. Voltage signals Vdc/2 and |vs | are compared to obtain signal Sc . When Vdc/2 > |vs |, Sc is a high value. On the contrary, Sc is a low value when Vdc/2 < |vs |. The output signal of the PWM circuit and signals Sb and Sc are sent to the mode selection circuit. The output of the mode selection circuit will generate the control signals of power electronic switches S2 and S3 according to Table I. The detected utility voltage is also sent to a comparator to obtain complementary square signals that are synchronous with the detected utility voltage. The complementary square signals are the control signals of the power electronic switches of the full-bridge inverter. As mentioned earlier, only two power electronic switches S2 or S3 in the five-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is Vdc/2. Therefore, the five-level inverter can reduce the switching loss effectively.

B. DC–DC Converter

Fig. 7 shows the control block of the dc–dc converter. The input of the dc–dc converter is the output of the solar cell array. A ripple voltage with a frequency double that of the utility will appear in the dc bus voltage Vdc, while the five-level inverter injects real power into the utility. The function of MPPT will be degraded, while the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltage superimposed on the dc bus voltage Vdc must be blocked by the dc–dc converter for improving the function of MPPT. Accordingly, the dual control loops, an outer voltage control loop, and an inner current control loop are applied to control the dc–dc converter. Since the output voltage of the dc–dc converter is the dc bus voltage that is controlled to be a constant voltage by the five-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop is applied to control the inductor current to approach a constant current to block the ripple voltage of dc bus voltage Vdc. The perturbation and observation method is adopted to obtain the function of MPPT [24], and it is incorporated into the controller of the dc–dc converter. The output of the MPPT controller is the desired output voltage of the solar cell array, and it is the reference voltage of the outer voltage control loop. The output voltage of the solar cell array is perturbed first, and then the output power variation of the solar cell array is observed to determine the next perturbation for the output voltage of the solar cell array. The output power of the solar cell array is calculated from the product of the output voltage of the solar cell array and the inductor current. Therefore, the output voltage of the solar cell array and the inductor current are
detected and sent to a MPPT controller to determine the desired output voltage of the solar cell array. The detected output voltage and desired output voltage of the solar cell array are sent to a subtractor, and the subtracted result is sent to a P-I controller. The output of the P-I controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the dc–dc converter. For protecting the renewable power generation system from the voltage rise, the MPPT function will be disabled and the power electronic switch S1 will be turned OFF when the inverter stage is interrupted after detecting the islanding operation. Therefore, the output voltage of solar cell array is limited to the open-circuit voltage of solar cell array, and the dc bus voltage $V_{dc}$ is also limited.

Fig. 6. Control block diagram of five-level inverter.

<table>
<thead>
<tr>
<th>Solar module</th>
<th>Rate of maximum power</th>
<th>75W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open voltage</td>
<td></td>
<td>21V</td>
</tr>
<tr>
<td>Short current</td>
<td></td>
<td>5.0A</td>
</tr>
<tr>
<td>DC–DC converter</td>
<td></td>
<td>470pF</td>
</tr>
<tr>
<td>Inductor ($L_2$)</td>
<td></td>
<td>2mH</td>
</tr>
<tr>
<td>Switch frequency</td>
<td></td>
<td>25kHz</td>
</tr>
</tbody>
</table>

### Five-level inverter
- DC bus capacitor ($C_1$ and $C_2$) | | 2200μF |
- Filter inductor ($L_1$) | | 1.4mH |
- DC bus setting voltage | | 150V |
- Switch frequency (PWM) | | 25kHz |
- Utility voltage | | 110V |
- Utility frequency | | 60Hz |

Fig. 7. Control block of the dc–dc converter

Fig. 16. Circuit configuration of the developed photovoltaic power generation system with the function of supplying reactive power

Fig. 17. Control block diagram of five-level inverter with the function of supplying reactive power.
VII. Result

![Simulation Model Diagram](image)

Fig. 7.1 Simulation model diagram

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Fig. 7.2 Experimental results of the five-level inverter. (a) Utility voltage. (b) Output current of the five-level inverter. (c) DC capacitor voltage $V_C_2$. (d) DC capacitor voltage $V_C_3$.

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Fig. 7.3. Experimental results for full-bridge inverter of the five-level inverter. (a) Output current of the full-bridge inverter $i_o$. (b) Input current of the full-bridge inverter $i_dc$. (c) Driver signal of $S_4$. (d) Driver signal of $S_5$.

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Fig. 7.4. Experimental results of the five-level inverter. (a) Utility voltage. (b) Output voltage of the full-bridge inverter. (c) Output voltage of the dual-buck converter.

---

Fig. 7.5. Experimental results for the dc–dc converter of the developed photovoltaic power generation system. (a) Voltage ripple of dc capacitor $C_2$. (b) Voltage ripple of dc capacitor $C_3$. (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc converter.

---

Fig. 7.6. Experimental results for the developed photovoltaic power generation
system under the distorted utility voltage. (a) Utility Voltage. (b) Output current of the five-level inverter.

**Extension circuit and outputs**

![Fig 7.7 simulation model diagram for Photovoltaic Power generation five level inverter](image)

![Fig. 7.8. Experimental results for the dc–dc converter of the developed photovoltaic power generation system. (a) Voltage ripple of dc capacitor C2. (b) Voltage ripple of dc capacitor C3. (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc](image)

![Fig. 7.9. Experimental results for the developed photovoltaic power generation system under the distorted utility voltage. (a) Utility Voltage. (b) Output current of the five-level inverter.](image)

**CONCLUSION**

A photovoltaic power generation system with a five-level inverter is developed in this paper. The five-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation. The Simulation results verify the developed photovoltaic power generation system, and the five-level inverter achieves the expected performance.

**REFERENCES**


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Space Vector Pulse Width Amplitude Modulation for a Buck–Boost Voltage Source Five Level Inverter

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Abstract

This project proposes a space vector pulse width amplitude modulation (SVPWAM) method for a buck–boost voltage source five level inverter. The switching loss is reduced by 87%, compared to a conventional sinusoidal pulse width modulation (SPWM) method. For a current source inverter, the switching loss is reduced by 60%. In both cases, the power density is increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM, by only using one-third switching frequency of the latter one. A 1-kW boost-converter-inverter prototype has been built and tested using this modulation method. The maximum overall system efficiency of 96.7% has been attained at full power rating. The whole system power density reaches 2.3 kW/L and 0.5 kW/lb. The numbers are remarkable at this power rating. As a result, it is feasible to use SVPWAM to make the buck–boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost. Such applications include electric vehicle motor drive or engine starter/alternator.

I. Introduction

Currently, two existing inverter topologies are used for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional three-phase inverter with a high voltage battery and a three-phase pulsedwidth modulation (PWM) inverter with a dc/dc boost front end. The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor’s constant power speed range (CPSR), which can be alleviated through the dc–dc boosted PWM inverter.

Fig. 1.1 shows a typical configuration of the series plug-in electric vehicle (PHEV). The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed. Active switching rectifier or a diode rectifier with small DC link capacitor have been proposed.
Fig. 1.1. Typical configuration of a series PHEV

II. SPACE VECTOR MODULATION

2.1 Introduction

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM). It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

2.2 Principle

A three-phase inverter as shown to the right converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. i.e. if A⁺ is on then A⁻ is off and vice versa. This leads to eight possible switching vectors for the inverter, V₀ through V₇ with six active switching vectors and two zero vectors.

III. SVPWAM FOR VSI

3.1 Principle of SVPWAM Control in VSI

The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig. 2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all.

Fig. 2.1. Topology of a basic three phase inverter.

Fig. 3.1. SVPWAM for VSI.

Fig. 3.2. DC-link voltage of SVPWAM in VSI.
The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore, S1 and S2 keep constant ON, and S3 and S6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage \( V_{ac} \) at this time. Consequently, the dc-link voltage should present a \( 6\omega \) varied feature to maintain a desired output voltage. The corresponding waveform is shown in solid line in Fig. 3.2. A dc–dc conversion is needed in the front stage to generate this \( 6\omega \) voltage. The topologies to implement this method will be discussed later. The original equations for time period \( T_1 \) and \( T_2 \) are

\[
T_1 = \frac{\sqrt{3}}{2} m \sin \left( \frac{\pi}{3} - \theta \right); \quad T_2 = \frac{\sqrt{3}}{2} m \sin \theta
\]

where \( \theta \in [0, \pi/3] \) is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics.

Fig. 3.3. Vector placement in each sector for VSI.

![Vector placement in each sector for VSI](image)

Fig. 3.4. Theoretic waveforms of dc-link voltage, output line-to-line voltage and switching signals.

Therefore, in order to keep the switching period constant but still keep the same pulsewidth as the original one, the new time periods can be calculated as

\[
\frac{T_1'}{T_2'} = \frac{T_1}{T_1 + T_2}
\]

The vector placement within one switching cycle in each sector is shown in Fig. 3.3. Fig. 3.4 shows the output line-to-line voltage and the switching signals of S1.

### 3.2 Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within \([-60^\circ, 60^\circ]\), at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage \( V_{DC} \), and the current stress is equal to output current \( i_a \). Thus the switching loss for each switch is

\[
P_{SW,i} = \frac{1}{2\pi} \int_{-\pi/6}^{\pi/6} \frac{E_{SR} |I_m \sin(\omega t)| \cdot V_{DC}}{V_{ref}I_{ref}} \cdot f_{sw} \, dt + \frac{\pi}{2} \cdot \frac{V_{DC}}{V_{ref}I_{ref}} \cdot E_{SR} \cdot f_{sw}
\]

where \( E_{SR} \), \( V_{ref} \), and \( I_{ref} \) are the references.
Since the SVPWAM only has PWM switching in two 60° sections, the integration over $2\pi$ can be narrowed down into integration within two 60° sections:

$$P_{SW,1} = \frac{2\sqrt{3}}{\pi} \cdot \left( I_m V_{DC} / (V_{ref} I_{ref}) \right) \cdot E_{SR} \cdot f_{sw}.$$  

The switching loss for a conventional SPWM method is

$$P_{SW,SPWM} = \frac{2}{\pi} \cdot \left( I_m V_{DC} / (V_{ref} I_{ref}) \right) \cdot E_{SR} \cdot f_{sw}.$$  

In result, the switching loss of SVPWAM over SPWM is $f = 13.4\%$. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases as Fig. 3.3 shows. As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 30%. In conclusion, SVPWAM can bring the switching loss down by 30–87%.

### 3.3 Principle of SVPWAM in CSI

The principle of SVPWAM in CSI is also to eliminate the zero vectors. As shown in Fig. 3.6, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are conducting together at any moment. Thus, for each switch, it only needs to do PWM switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selected in each sector, this method brings down the switching frequency by one-third.

![Fig. 3.6. Conventional CSI and its corresponding SVPWAM diagram.](image)

Fig. 3.6. Conventional CSI and its corresponding SVPWAM diagram.

Similarly, the dc-link current in this case is a 60° varied current. It is the maximum envelope of six output currents: $I_a, I_b, I_c, -I_a, -I_b, -I_c$, as shown in Fig. 3.8.

![Fig. 3.7. Switching voltage and current when pf = 1.](image)

Fig. 3.7. Switching voltage and current when pf = 1.

![Fig. 3.8. Vector placement for each sector for CSI.](image)

Fig. 3.8. Vector placement for each sector for CSI.

Similarly, the dc-link current in this case is a 60° varied current. It is the maximum envelope of six output currents: $I_a, I_b, I_c, -I_a, -I_b, -I_c$, as shown in Fig.
3.7. For example, in sector I, S1 always keeps ON, so the dc-link current is equal to Ia. The difference between dc-link current in CSI and dc-link voltage in VSI is dc-link current in CSI is overlapped with the phase current, but dc-link voltage in VSI is overlapped with the line voltage, not the phase voltage.

The time intervals for two adjacent vectors can be calculated in the same way as (1) and (2). According to diagram in Fig. 3.6, the vector placement in each switching cycle for six switches can be plotted in Fig. 3.8. The SVPWAM is implemented on conventional CSI through simulation. Fig. 3.9 shows the ideal waveforms of the dc current Idc, the output phase ac current and the switching signals of S1. The switching signal has two sections of PWM in positive cycle, but no PWM in negative cycle at all.

3.4 Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dc-link current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig. 3.7. Thus, the switching loss for a single switch is determined by

$$P_{SW_{-CSI}} = \frac{2}{\pi} \sqrt{3} I_{dc} \cdot \frac{V_l}{V_{ref}} \cdot E_{SR} f_{sw}.$$

When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result in (6). The corresponding switching loss ratio between SVPWAM and discontinuous SVPWM is shown in Fig. 3.10.

3.6 Spectrum Analysis Of Svpwam

A fair comparison in switching loss should be based on an equal output harmonics level. Thus, the switching loss may not be reduced if the switching frequency needs to be increased in order to compensate the harmonics. For example, discontinuous SVPWM has to have double switching frequency to achieve the same THD as continuous PWM. So the switching loss reduction is much smaller than 30%. Therefore, for the newly proposed SVPWAM, a spectrum analysis is conducted to be compared with other methods on the basis of an equal average switching frequency, which has not been considered in paper.
3.7 Spectrum Comparison Between SVPWAM, SPWM, and SVPWM

The object of spectrum analysis is the output voltage or current before the filter. The reason is that certain orders of harmonics can be eliminated by sum of switching functions in VSI or subtraction of switching functions in CSI. The comparison is between SVPWAM, DPWM, and continuous SVPWM in VSI/CSI. The switching frequency selected for each method is different, because the comparison is built on an equalized average switching frequency over a whole fundamental cycle, in order to make the harmonics comparable at both low modulation and high modulation range. Assume that the base frequency is $f_0 = 10.8$ kHz. Thus, $3f_0$ should be selected for SVPWAM, and $f_0$ should be selected for continuous SVPWM in VSI. In CSI, $3f_0$, $2f_0$, and $f_0$ should be selected for SVPWAM, discontinuous SVPWM, and continuous SVPWM, respectively.

Fig. 3.11. Spectrum of SPWM at switching frequency.

Fig. 3.12. Spectrum of discontinuous SVPWM at switching frequency.

The modulation index selected here is the maximum modulation index 1.13, since the SVPWAM always only has the maximum modulation index. Theoretically, the THD varies with modulation index. The dc-link voltage is designed to be a constant for SVPWM and an ideal 6ω envelope of the output six line-to-line voltages for SVPWAM. Thus, the harmonic of the SVPWAM here does not contain the harmonics from the dc–dc converter output. It is direct comparison between two modulation methods from mathematics point of view. Figs. 3.11–3.13 show the calculated spectrum magnitude at first side band of switching frequency range for three methods. It can be concluded that the ideal switching function of SVPWAM has less or comparable harmonics with SPWM and DPWM.

3.8 Analytical Double Fourier Expression for SVPWAM

The expression of double Fourier coefficient is

$$ A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} I_d e^{j(m_x x + n_y y)} dx dy $$

Fig. 3.13. Spectrum of SVPWAM at switching frequency.
TABLE I INTEGRATION LIMIT FOR LINE-TO-LINE VOLTAGE $V_{ab}(t)$

<table>
<thead>
<tr>
<th>$x(0)$</th>
<th>$y(0)$</th>
<th>$x(0)$</th>
<th>$y(0)$</th>
<th>Intc</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$\frac{\pi}{3}$</td>
<td>$\frac{\pi}{3}$</td>
<td>$\frac{\pi}{3}$</td>
<td>0</td>
</tr>
<tr>
<td>$\frac{2\pi}{3}$</td>
<td>$2\pi$</td>
<td>$\frac{\pi}{2}$</td>
<td>$\frac{\pi}{2}$</td>
<td>0</td>
</tr>
<tr>
<td>$\frac{2\pi}{3}$</td>
<td>$\frac{4\pi}{3}$</td>
<td>$\frac{\pi}{2}$</td>
<td>$\frac{\pi}{2}$</td>
<td>$\frac{\pi}{2}$</td>
</tr>
<tr>
<td>$\frac{2\pi}{3}$</td>
<td>$0$</td>
<td>$\frac{\pi}{2}$</td>
<td>$\frac{\pi}{2}$</td>
<td>$\frac{\pi}{2}$</td>
</tr>
</tbody>
</table>

where $y \in [0, 2\pi]$ represents the fundamental cycle; $x \in [0, 2\pi]$ represents one switching cycle. The double Fourier expression coefficients can be derived as long as the rising edge of each PWM waveform is known. The output line-to-line voltage $V_{ab}$ is used as an illustrative example. It is a function of switching function

$$V_{ab}(t) = V_{dc}(S_1(t) - S_3(t)).$$

So its double Fourier equation is equal to the subtraction of two double fourier equations for switching functions. The integration limits for $V_{ab}(t)$ is shown in Tables I. The coefficients finally could be simplified into a closed-form expression in terms of Bessel functions, which will not be discussed here.

3.9 Topologies For SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a 60 varied dc-link voltage or current; VSI or CSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter. The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current $I_{pn}$ to have a constant average value, the open zero state duty cycle $D_{op}$ will be regulated instantaneously to control $I_{pm}$ to have a 60 fluctuate average value, resulting in a pulse type 60 waveform at the real dc-link current $I_{pn}$, since $I_1$ is related to the input dc current $I_{in}$ by a transfer function

$$I_1 = \frac{1 - D_{op}}{1 - 2D_{op}} I_{in}$$

Fig. 3.14. SVPWAM-based boost-converter-inverter motor drive system.

IV.SIMULATION RESULTS

4.1 Variable DC-Link SPWM Control at High Frequency

When the output needs to operate at a relative high frequency, like between 120 Hz and 1 kHz, it is challenging to obtain a 60 dc-link voltage without increasing the
switching frequency of a boost converter. Because the controller does not have enough bandwidth. Furthermore, increasing boost converter switching frequency would cause a substantial increase of the total switching loss, because it takes up more than 45% of the total switching loss. The reason is because it switches at a complete current region. Also a normal SPWM cannot be used in this range because the capacitor is designed to be small that it cannot hold a constant dc link voltage. Therefore, the optimum option is to control the dc link voltage to be $6\omega$ and do a variable dc link SPWM modulation, as explained in Fig. 4.4. In this variable dc-link SPWM control, in order to get better utilization of the dc-link voltage, an integer times between the dc-link fundamental frequency and output frequency is preferred. When the output frequency is in [60 Hz, 120 Hz], a $6\omega$ dc link is chosen; when the frequency is in [120 Hz, 240 Hz], a $3\omega$ dc link is chosen; when the frequency is in [240 Hz, 360 Hz], a $2\omega$ dc link is chosen. A 1-kW boost-converter inverter prototype has been built in the laboratory to implement the SVPWAM control at 60 Hz and SPWM control at 1 kHz, in order to demonstrate their merits in reducing power loss and reducing the size compared to traditional methods. The picture of the hardware is shown in Fig. 4.4. It includes a DSP board, a gate drive board, a boost converter, a three-phase inverter, heat sink, and a fan cooling system. The dimension is 11 cm × 8 cm × 5 cm, and the total weight is 1.5 lb.

![Fig 4.1 simulation model diagram](image)

The parameters used in the test are rated power: 1 kW; battery voltage: 100–200 V; rated line voltage rms: 230 V; dc-link voltage peak: 324 V; switching frequency: 20 kHz; output frequency: 60 Hz–1 kHz
Fig. 4.2. Output voltage and input current at $V_{in} = 20\, V$, $V_{dc\, avg} = 60\, V$, $V_{lrms} = 46\, V$, $P_o = 40\, W$, $f_o = 60\, Hz$, $f_{sw} = 20\, kHz$.

Fig. 4.3. Output voltage and input current at $V_{in} = 100\, V$, $V_{dc\, avg} = 300\, V$, $V_{lrms} = 230\, V$, $P_o = 1\, kW$, $f_o = 60\, Hz$, $f_{sw} = 20\, kHz$.

4.2 SVPWAMBuck–Boost Voltage Source Five level Inverter

Fig 4.6: simulated five level model diagram

Fig. 4.4. Output voltage and input current
V. Conclusion
The SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method. 1) The switching power loss is reduced by 90% compared with the voltage changes from 0 to full rating at 300 V: (a) SVPWAM, (b) SPWM. increases from 0 to full rating under two methods. Since the research target is only inverter, the test condition is based on varying the output power by changing output voltage from 0 to 230 V. It is observed that in the SVPWAM method, conduction loss accounts for 80% of the total power loss, but in the SPWM method, switching loss is higher than conduction loss. The switching loss is reduced from 10 to 1.4 W from SPWM to SVPWAM. An estimated 87% switching loss reduction has been achieved. 2) The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6 μF) and small heat sink is needed. 3) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress. A high-efficiency, high-power density, high-temperature, and low-cost 1-kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses has been validated by the experimental results that were obtained from the laboratory scale prototype.

References
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SRAM Cells Using Test Vector Monitoring in BIST Architecture for SOC

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Abstract—Input vector monitoring concurrent built-in self test (BIST) schemes perform testing during the normal operation of the circuit without imposing a need to set the circuit offline to perform the test. These schemes are evaluated based on the hardware overhead and the concurrent test latency (CTL), i.e., the time required for the test to complete, whereas the circuit operates normally. In this brief, we present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff.

I. Introduction

Built-in self test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage, whereas simultaneously they relax the reliance on expensive external testing equipment. Hence, they constitute an attractive solution to the problem of testing VLSI devices [1]. BIST techniques are typically classified into offline and online. Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV). Therefore, to perform the test, the normal operation of the CUT is stalled and, consequently, the performance of the system in which the circuit is included, is degraded. Input vector monitoring concurrent BIST techniques [2]–[10] have been proposed to avoid this performance degradation. These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT; if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig. 1. The CUT has $n$ inputs and $m$ outputs and is tested exhaustively; hence, the test set size is $N = 2^n$. The technique can operate in either normal or test mode, depending on the value of the signal labeled $T/N$.

During normal mode, the vector that drives the inputs of the CUT (denoted by $d[n:1]$ in Fig. 1) is driven from the normal input vector ($A[n:1]$). $A$ is also driven to a concurrent BIST unit (CBU), where it is compared with the active test set. If it is found that a hit has occurred. In this case, is removed from the active test set and the signal response verifier enable (rve) is issued, to enable the $m$-stage RV to capture the CUT response to the input vector [1]. When all input vectors have performed hit, the contents of RV are examined. During test mode, the inputs to the CUT are driven from the CBU outputs denoted $TG[n:1]$. The concurrent test latency (CTL) of an input
vector monitoring scheme is the mean time (counted either in number of clock cycles or time units) required to complete the test while the CUT operates in normal mode.

II. Testing

The electronics technology accomplished higher levels of integration into a single silicon chip that led to Large Scale Integration (LSI), which preceded VLSI, the applications of electronic systems have experienced an almost unlimited expansion. However, despite the many advantages provided by VLSI, the inherent high integration level started to necessitate very sophisticated testing strategies in order to verify the correct device operation. As the electronics market stimulated the use of VLSI in a variety of tasks from critical military applications to consumer products, the reliability of the products’ functioning gained an escalating importance. The expanding demand for ASIC applications led to development of more sophisticated Computer Aided Design (CAD) tools; which have shown most significant progress in layout and simulation, with yet more inferior improvement in testing. This consequently leads to designs with superior complexity, but which are in contrast extremely difficult to test effectively. Moreover, due to the low volume attribute of ASICs, the high test costs cannot be retaliated with large amounts of mass production. Thereupon, despite the traditional design point of view, that design and test can be considered as two different aspects of development, current design processes consider testing as an integral part of design rather than design and test being two mutually exclusive processes. At present, as the number of gates per chip exceeds millions, not only the design process is resolutely bound to the designed circuits’ being testable, but also some percentage of auxiliary device circuitry is intentionally included on devices, in order to assure the functionality of the “actual” circuit is verified to an adequate level. The two concepts mentioned in the last argument, the former leading to Design for Testability (DfT) Tests are applied at several steps in the hardware manufacturing flow and, for certain products, may also be used for hardware maintenance in the customer’s environment. The tests generally are driven by test programs that execute in Automatic Test Equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. In addition to finding and indicating the presence of defects (i.e., the test fails), tests may be able to log diagnostic information about the nature of the encountered test fails. The diagnostic information can be used to locate the source of the failure.

The most common method for delivering test data from chip inputs to internal circuits under test (CUTs, for short), and observing their outputs, is called scan-design. In scan-design, registers (flip-flops or latches) in the design are connected in one or more scan chains, which are used to gain access to internal nodes of the chip. Test patterns are shifted in via the scan chain(s), functional clock signals are pulsed to test the circuit during the "capture cycle(s)", and the results are then shifted out to chip output pins and compared against the expected "good machine" results.

Before proceeding to the details of testing, it is imperative to describe certain terms related to digital circuit testing. The three terms, which are used to define the test data are:
(i) Input test vector (input vector/test vector): Applied parallel binary signals to the circuit under test via the available primary inputs, at one instance. For example, Testing and Built in Self Test 10 for a circuit with 8 primary inputs, 10001010 might be one of the applied input test vectors.

(ii) Test Pattern: Applied test vector plus the fault free outputs observed from the available parallel primary outputs. For example, for the above hypothesized circuit with 4 primary outputs, if the fault free outputs are 1111 for primary inputs 10001010, the test pattern is 10001010 1111.

(iii) Test Set: The complete set of all test patterns applied to the circuit under test to determine its non-faulty operation. The test set comprises all the sequence of applied test vectors and to be observed non-fault outputs.

III. BIST

Built-in Self Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to.

The main drivers for the widespread development of BIST techniques are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed-signal testers that possess special digital and analog testing capabilities. BIST can be used to perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high-end testers.

Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated. Better fault coverage, since special test structures can be incorporated onto the chips. Shorter test times if the BIST can be designed to test more structures in parallel. Easier customer support. Capability to perform tests outside the production electrical testing environment.

Built-in self-test (BIST) has been proven to be one of the most cost-effective and the last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

This technique does not detect any real-time errors but is widely used in the industry for testing the functional circuitry at the system, board, or chip level to ensure product quality. Functional offline BIST performs a test based on the functional specification of the functional circuitry and often employs a functional or high-level fault model. Normally such a test is implemented as diagnostic software or firmware. Structural offline BIST performs a test based on the structure of the functional circuitry. There are two general classes of structural offline BIST techniques: (1) external BIST, in which test pattern
generation and output response analysis is done by circuitry that is separate from the functional circuitry being tested, and (2) internal BIST, in which the functional storage elements are converted into test pattern generators and output response analyzers. Some external BIST schemes test sequential logic directly by applying test patterns at the inputs and analyzing the responses at its outputs. Fig 5.2 shows a typical logic BIST system using the structural offline BIST technique. The test pattern generator (TPG) automatically generates test patterns for application to the inputs of the circuit under test (CUT). The output response analyzer (ORA) automatically compacts the output responses of the CUT into a signature. Specific BIST timing control signals, including scan enable signals and clocks, are generated by the logic BIST controller for coordinating the BIST operation among the TPG, CUT, and ORA. The logic BIST controller provides a pass/fail indication once the BIST operation is complete. It includes comparison logic to compare the final signature with an embedded golden signature, and often comprises diagnostic logic for fault diagnosis. As compaction is commonly used for output response analysis, it is required that all storage elements in the TPG,

**IV. SRAM operation**

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

**V. PROPOSED SCHEME**

Let us consider a combinational CUT with n input lines, as shown in Fig.5.2; hence the possible input vectors for this CUT are 2^n. The proposed scheme is based on the idea of monitoring a window of vectors, whose size is W, with W = 2^w, where w is an integer number w < n. Every moment, the test vectors belonging to the window are monitored, and if a vector performs a hit, the RV is enabled. The bits of the input vector are separated into two distinct sets comprising w and k bits, respectively, such that w + k = n. The k (high order) bits of the input vector show whether the input vector belongs to the window under consideration. The w remaining bits show the relative location of the incoming vector in the current window. If the incoming vector belongs to the current window and has not been received during the examination of the current window, we say that the vector has performed a hit and the RV is clocked to capture the CUT’s response to the vector. When all vectors that belong to the current window have reached the CUT inputs, we proceed to examine the next window.

![Fig 3.2 L-BIST Architecture](image-url)
The module implementing the idea is shown in Fig.5. 2. It operates in one out of two modes, normal, and test, depending on the value of the signal T/N. When T/N = 0 (normal mode) the inputs to the CUT are driven by the normal input vector. The inputs of the CUT are also driven to the CBU as follows: the k (high order) bits are driven to the inputs of a k-stage comparator; the other inputs of the comparator are driven by the outputs of a k-stage test generator TG. The proposed scheme uses a modified decoder (denoted as m_dec in Fig.5. 2) and a logic module based on a static-RAM (SRAM)-like cell, as will be explained shortly. The design of the m_dec module for w = 3 is shown in Fig.5. 3 and operates as follows. When test generator enable (tge) is enabled, all outputs of the decoder are equal to one. When comparator (cmp) is enabled, all outputs of the decoder are equal to one. When comparator (cmp) is disabled (and tge is not enabled) all outputs are disabled.

When tge is disabled and cmp is enabled, the module operates as a normal decoding structure. The architecture of the proposed scheme for the specific case n = 5, k = 2, and w = 3, is shown in Fig.5. 4. The module labeled logic in Fig.5. 4 is shown in Fig.5. 5. It comprises W cells (operating in a fashion similar to the SRAM cell), a sense amplifier, two D flip-flops, and a w-stage counter (where w = log2W). The overflow signal of the counter drives the tge signal through a unit flip-flop delay. The signals clk_ and clock (clk) are enabled during the active low and high of the clock, respectively. In the sequel, we have assumed a clock that is active during the second half of the period, as shown in Fig.5. 5.
Fig. 5. Design of the logic module.

In the sequel, we describe the operation of the logic module, presenting the following cases: 1) reset of the module; 2) hit of a vector (i.e., a vector belongs in the active window and reaches the CUT inputs for the first time); 3) a vector that belongs in the current window reaches the CUT inputs but not for the first time; and 4) the operation (i.e., all cells of the window are filled and we will proceed to examine the next window).

A. Reset of the Module
At the beginning of the operation, the module is reset through the external reset signal. When reset is issued, the tge signal is enabled and all the outputs of the decoder (Fig. 5.3) are enabled. Hence, DA1, DA2, . . . , DAW are one; furthermore, the CD_ signal is enabled; therefore, a one is written to the right hand side of the cells and a zero value to the left hand side of the cells.

B. Hit of Vector (i.e., Vector Belongs in the Active Window and Reaches the CUT Inputs for the First Time) During normal mode, the inputs to the CUT are driven from the normal inputs. The n inputs are also driven to the CBU as follows: the w low-order inputs are driven to the inputs of the decoder; the k high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (clk_ and cmp are enabled) the addressed cell is read; because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop (the one whose clock input is inverted) enables the AND gate (whose other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.

C. Vector That Belongs in the Current Window Reaches the CUT Inputs But Not for the First Time
If the cell corresponding to the incoming vector contains a one (i.e., the respective vector has reached the CUT inputs during the examination of the current window before), the rve signal is not enabled during the first half of the clock cycle; hence, the w-stage counter is not triggered and the AND gate is not enabled during the second half of the clock cycle.

D. the Operation (i.e., All Cells of the Window are Filled and We Will Proceed to Examine the Next Window)
When all the cells are full (value equal to one), then the value of the w-stage counter is all one. Hence, the activation of the rve signal causes the counter to overflow; hence in the next clock cycle (through the unit flop delay) the tge signal is enabled and all the cells (because all the outputs of the decoder of Fig. 5.3 are enabled) are set to zero.

When switching from normal to test mode, the w-stage counter is reset. During test mode, the w-bit output of the counter is
applied to the CUT inputs. The outputs of the counter are also used to address a cell. If the cell was empty (reset), it will be filled (set) and the RV will be enabled. Otherwise, the cell remains full and the RV is not enabled.

VI. CONCLUSION
BIST schemes constitute an attractive solution to the problem of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can circumvent problems appearing in offline BIST techniques. The evaluation criteria for this class of schemes are the hardware overhead and the CTL, i.e., the time required for the test to complete, while the circuit operates normally. In this brief, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

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